XD6130/XD6131 Series

ETR02039-006a

Watchdog Timeout Period Externally Adjustable Voltage Detector

☆AEC-Q100 Grade1

■ GENERAL DESCRIPTION

The XD6130/XD6131 series are voltage detectors with a watchdog function. The watchdog timeout time and release delay time can be set as desired using a single external capacitor. These voltage detectors are used for microprocessor monitoring, and when the power voltage reaches the detect voltage or an L→H pulse is not input to the watchdog pin within the watchdog timeout time, an L level signal is output from the RESETB pin.

The XD6130 series has a manual reset function. When the manual reset pin is set to Low level at any desired timing, an L level signal is output from the RESETB pin.

The XD6131 series has a watchdog ON/OFF function. By setting the EN pin to L level, the watchdog function can be turned OFF while the voltage detector that monitors the power voltage continues to operate.

The MRB pin and EN pin are pulled up internally to V_{IN}, and thus these pins can be left open when not used.

■APPLICATIONS

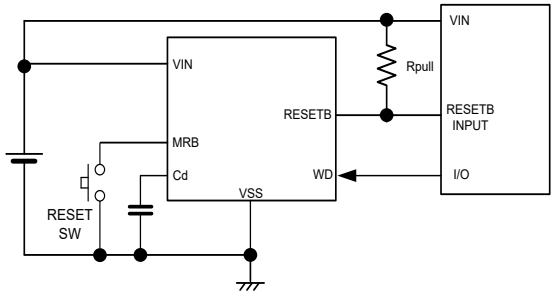
- ●Microprocessor reset and malfunction monitoring circuitry
- ●Memory battery backup circuits
- ●Power-on reset circuits
- ●Power failure detection

■FEATURES

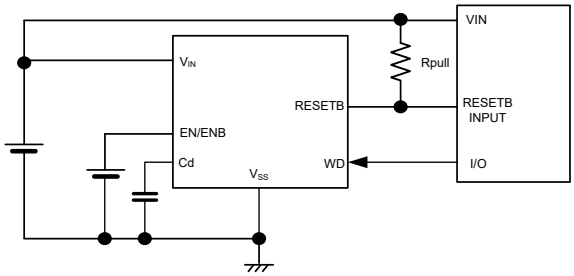
Operating Ambient Temperature	: -40℃ ~ 125℃
Operating Voltage Range	: 1.5V ~ 6.0V
Detect Voltage (Standard)	: 1.6V,2.2V,2.3V,2.4V,2.9V,3.0V, 3.1V,4.4V,4.5V,4.6V,±1.0%
Detect Voltage Range(Option)	: 1.6V ~ 5.0V (±1.0%)
Hysteresis Width	: V_{DFL}×5%
Temperature Characteristics	: ±50ppm/℃
Output Configuration	: N-channel open drain output
Low Power Consumption	: 8.1μA Detect 9.8μA Release 2.5μA Release (EN=L)
Function	: Manual Reset (XD6130) : Watchdog function OFF (XD6131)
WD Timeout Time	: 100ms (Cd=0.1μF)
Release Delay Time	: 100ms (Cd=0.1μF) (at power on) 10ms (Cd=0.1μF) (After Watchdog Timeout)
Package	: SOT-26
Environmentally Friendly	: EU RoHS compliant, Pb free

■TYPICAL APPLICATION CIRCUIT

XD6130 Series



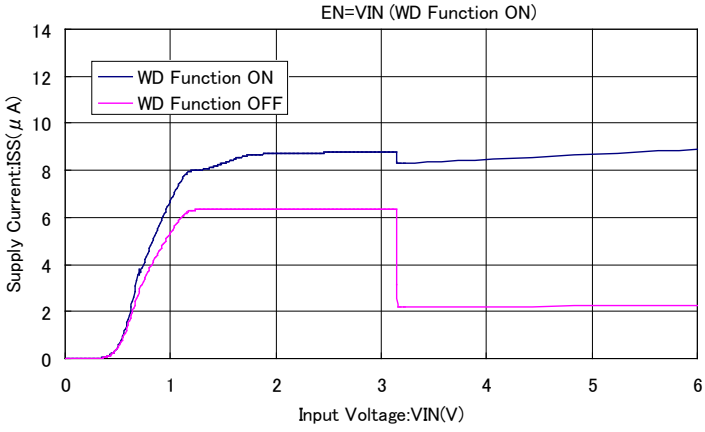
XD6131 Series



■TYPICAL PERFORMANCE CHARACTERISTICS

XD6131A301MR-Q

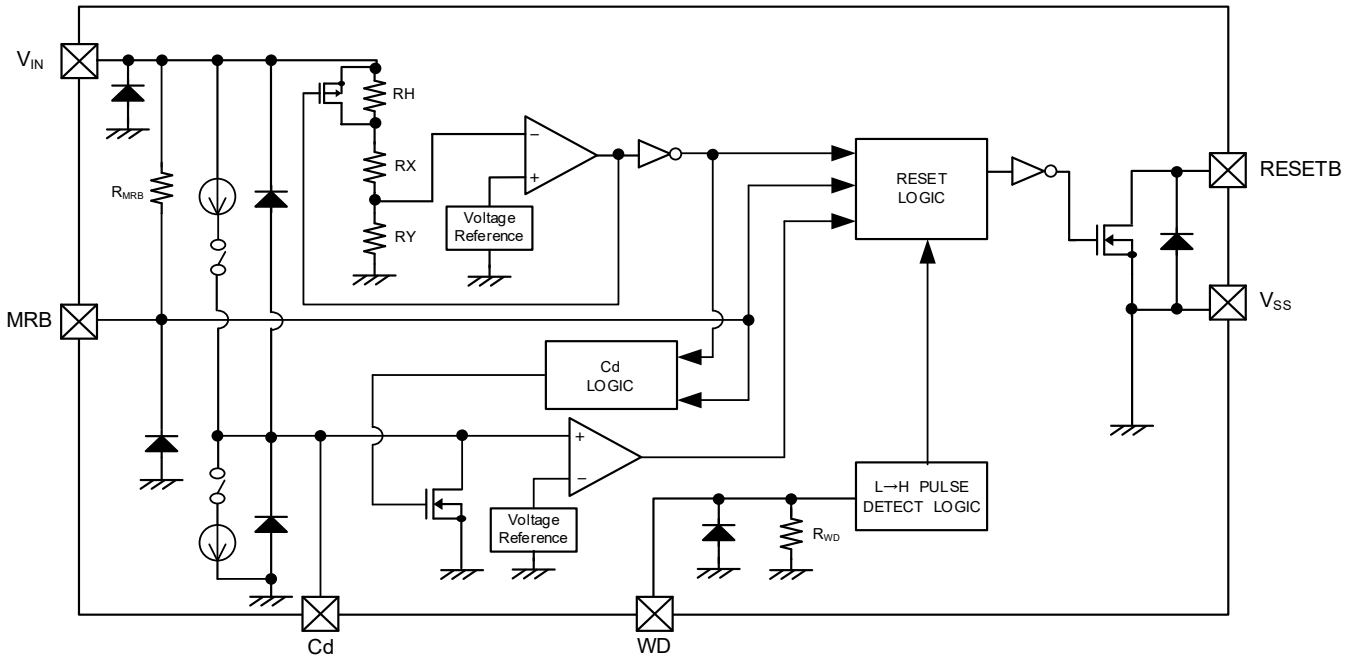
Cd=0.01μF, WD=RESETB=OPEN, Ta=25℃
EN=VSS(WD Function OFF)
EN=VIN (WD Function ON)



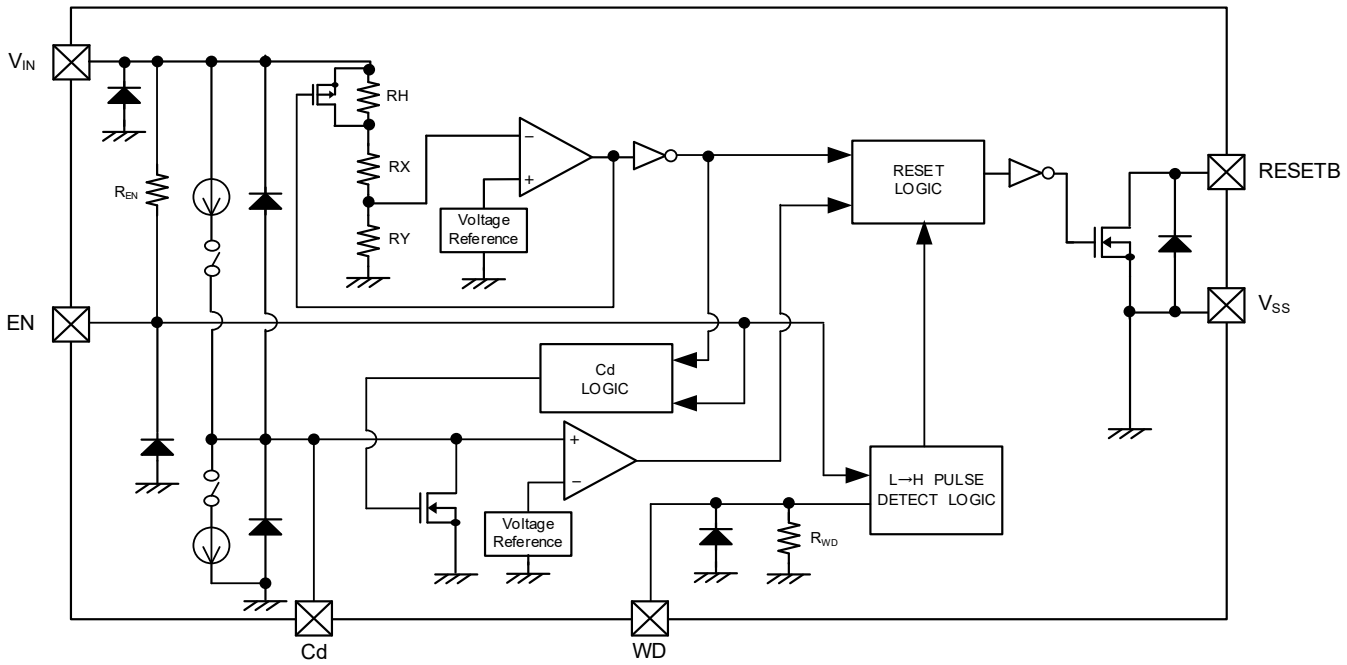
The above values do not include the current that flows to the EN pull-up resistance.

■BLOCK DIAGRAM

●XD6130 Series Type A



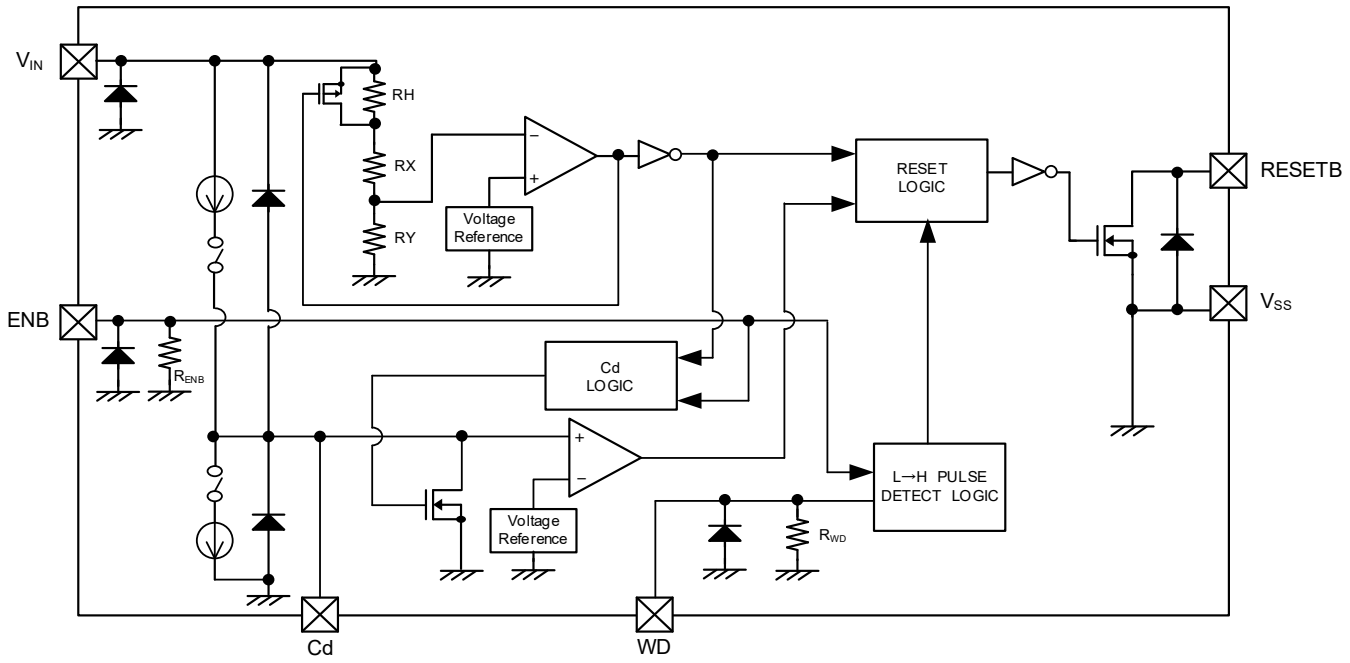
● XD6131 Series Type A



* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

■BLOCK DIAGRAM

● XD6131 Series Type B



* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

■PRODUCT CLASSIFICATION

●Ordering Information

XD6130①②③④⑤⑥-⑦

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	TYPE	A	MRB pin With pull-up resistor
②③	Detect Voltage	16 ~ 50	e.g. 1.6V → ②=1, ③=6
④	Detect Accuracy	1	±1.0%
⑤⑥-⑦ (*1)	Package (Order Unit)	MR-Q	SOT-26 (3000pcs/Reel)(*2)

(*1) The "-Q" suffix denotes "AEC-Q100" and "Halogen and Antimony free" as well as being fully EU RoHS compliant.

(*2) The SOT-26 reels are shipped in a moisture-proof packing.

XD6131①②③④⑤⑥-⑦

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	TYPE	A	EN pin With pull up resistor
		B	ENB pin With pull down resistor
②③	Detect Voltage	16 ~ 50	e.g. 1.6V → ②=1, ③=6
④	Detect Accuracy	1	±1.0%
⑤⑥-⑦ (*1)	Package (Order Unit)	MR-Q	SOT-26 (3000pcs/Reel)(*2)

(*1) The "-Q" suffix denotes "AEC-Q100" and "Halogen and Antimony free" as well as being fully EU RoHS compliant.

(*2) The SOT-26 reels are shipped in a moisture-proof packing.

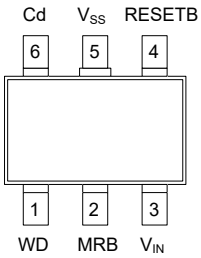
●Detect Voltage (Standard)

Part No.	TYPE	Detect Voltage
XD6130A161MR-Q	MRB pin With pull-up resistor	1.6V
XD6130A221MR-Q		2.2V
XD6130A231MR-Q		2.3V
XD6130A241MR-Q		2.4V
XD6130A291MR-Q		2.9V
XD6130A301MR-Q		3.0V
XD6130A311MR-Q		3.1V
XD6130A441MR-Q		4.4V
XD6130A451MR-Q		4.5V
XD6130A461MR-Q		4.6V

Part No.	TYPE	Detect Voltage
XD6131A161MR-Q	EN pin With pull-up resistor	1.6V
XD6131A221MR-Q		2.2V
XD6131A231MR-Q		2.3V
XD6131A241MR-Q		2.4V
XD6131A291MR-Q		2.9V
XD6131A301MR-Q		3.0V
XD6131A311MR-Q		3.1V
XD6131A441MR-Q		4.4V
XD6131A451MR-Q		4.5V
XD6131A461MR-Q		4.6V
XD6131B161MR-Q	ENB pin With pull-down resistor	1.6V
XD6131B221MR-Q		2.2V
XD6131B231MR-Q		2.3V
XD6131B241MR-Q		2.4V
XD6131B291MR-Q		2.9V
XD6131B301MR-Q		3.0V
XD6131B311MR-Q		3.1V
XD6131B441MR-Q		4.4V
XD6131B451MR-Q		4.5V
XD6131B461MR-Q		4.6V

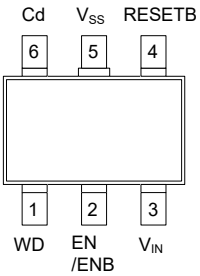
For another type of detect voltage, please contact your local Torex sales office or representative.
Output voltages can be set internally from 1.6V to 5.0V.

■PIN CONFIGURATION



SOT-26
(TOP VIEW)

XD6130 series



SOT-26
(TOP VIEW)

XD6131 series

■PIN ASSIGNMENT

XD6130 Series

PIN NUMBER	PIN NAME	FUNCTIONS
SOT-26		
1	WD	Watchdog Input
2	MRB	Manual Reset Input
3	V_{IN}	Power Input
4	RESETB	Reset Output
5	V_{SS}	Ground
6	Cd	Adjustable Pin for Release Delay Time/Watchdog Timeout

XD6131 Series

PIN NUMBER	PIN NAME	FUNCTIONS
SOT-26		
1	WD	Watchdog Input
2	EN	Watchdog ON/OFF Control (XD6131A)
	ENB	Watchdog ON/OFF Control (XD6131B)
3	V_{IN}	Power Input
4	RESETB	Reset Output
5	V_{SS}	Ground
6	Cd	Adjustable Pin for Release Delay Time/Watchdog Timeout

■FUNCTION CHART

1) XD6130 Series

V_{IN} *2	V_{MRB} *3	V_{WD} *6	V_{RESETB} *7
H	H	H	L⇔H
		L	
		OPEN	
		L⇔H	H
H	L	*1	L
L	L		L
	H		L

2) XD6131A Series

V_{IN} *2	V_{EN} *4	V_{WD} *6	V_{RESETB} *7
H	H	H	L⇔ H
		L	
		OPEN	
		L⇔ H	H
H	L	*1	H
L	L		L
	H		L

3) XD6131B Series

V_{IN} *2	V_{ENB} *5	V_{WD} *6	V_{RESETB} *7
H	L	H	L⇔ H
		L	
		OPEN	
		L⇔ H	H
H	H	* 1	H
L	L		L
	H		L

*1: Includes all WD logic (VWD=H, L, OPEN, H→L, L→H)

*2: V_{IN}=H indicates higher than the release voltage.
V_{IN}=L indicates lower than the detect voltage.

*3: V_{MRB}=H indicates MRB High Level Voltage.
V_{MRB}=L indicates MRB Low Level Voltage.
Since MRB pin of XD6130 Series is pulled up internally, the open condition of MRB pin is acceptable when MR function is not required.

*4: V_{EN}=H indicates EN High Level Voltage.
V_{EN}=L indicates EN Low Level Voltage.
The EN pin of the XD6131A Series is pulled up internally, enabling the WD function to be used with EN open.

*5: V_{ENB}=H indicates ENB High Level Voltage.
V_{ENB}=L indicates ENB Low Level Voltage.
The ENB pin of the XD6131B Series is pulled down internally, enabling the WD function to be used with ENB open.

*6: V_{WD}=H indicates WD High Level Voltage.
V_{WD}=L indicates WD Low Level Voltage.

*7: VRESETB=H indicates the release state.
VRESETB=L indicates the detect state.

■ ABSOLUTE MAXIMUM RATINGS

XD6130 Series

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	-0.3 ~ 7.0	V
WD Input Voltage		V_{WD}	-0.3 ~ 7.0	V
MRB Input Voltage		V_{MRB}	-0.3 ~ 7.0	V
Cd Pin Voltage		V_{Cd}	-0.3 ~ V_{IN}+0.3 or 7.0(*1)	V
Output Voltage		V_{RESETB}	-0.3 ~ 7.0	V
Cd Pin Current		I_{Cd}	10	mA
Output Current		I_{OUT}	30	mA
Power Dissipation (Ta=25℃)	SOT-26	Pd	250	mW
			600 (40mm x 40mm Standard Board) (*2)	
Operating Ambient Temperature		Topr	-40 ~ 125	℃
Storage Temperature		Tstg	-55 ~ 125	℃

All voltages are described based on the VSS pin.

(*1) The maximum value should be V_{IN}+0.3V or 7.0V in the lowest.

(*2) The power dissipation figure shown is PCB mounted and is for reference only.
Please refer to PACKAGING INFORMATION for the mounting condition.

XD6131 Series

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	-0.3 ~ 7.0	V
WD Input Voltage		V_{WD}	-0.3 ~ 7.0	V
EN/ENB Input Voltage		V_{EN}/V_{ENB}	-0.3 ~ 7.0	V
Cd Pin Voltage		V_{Cd}	-0.3 ~ V_{IN}+0.3 or 7.0(*1)	V
Output Voltage		V_{RESETB}	-0.3 ~ 7.0	V
Cd Pin Current		I_{Cd}	10	mA
Output Current		I_{OUT}	30	mA
Power Dissipation (Ta=25℃)	SOT-26	Pd	250	mW
			600 (40mm x 40mm Standard Board) (*2)	
Operating Ambient Temperature		Topr	-40 ~ 125	℃
Storage Temperature		Tstg	-55 ~ 125	℃

All voltages are described based on the VSS pin.

(*1) The maximum value should be V_{IN}+0.3V or 7.0V in the lowest.

(*2) The power dissipation figure shown is PCB mounted and is for reference only.
Please refer to PACKAGING INFORMATION for the mounting condition.

■ELECTRICAL CHARACTERISTICS

XD6130 Series

PARAMETER	SYMBOL	CONDITIONS		Ta=25℃			-40℃≦Ta≦125℃(*9)			UNITS	CIRCUIT
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Operating Voltage	V_{IN}			1.5	-	6.0	1.5	-	6.0	V	①
Detect Voltage	V_{DFL}	$V_{DF(T)}$(*1)=1.6~5.0V		$V_{DF(T)}$ ×0.99	$V_{DF(T)}$	$V_{DF(T)}$ ×1.01	$V_{DF(T)}$ ×0.975	$V_{DF(T)}$	$V_{DF(T)}$ ×1.025	V	
Temperature Characteristics	$\Delta V_{DFL}/(\Delta Topr \cdot V_{DFL})$	-40℃≦Topr≦125℃		-	±50	-	-	±50	-	ppm /℃	
Hysteresis Width	V_{HYS}			V_{DFL} ×0.04	V_{DFL} ×0.05	V_{DFL} ×0.06	V_{DFL} ×0.03	V_{DFL} ×0.05	V_{DFL} ×0.07	V	
Supply Current	Iss	$V_{IN}=V_{DF(T)}$ ×0.9		-	8.1	12.1	-	8.1	14.0	μA	②
		$V_{IN}=V_{DF(T)}$ ×1.1		-	9.8	12.6	-	9.8	13.6		
Output Current	I_{RBOUT}	N-ch. V_{RESETB}=0.3V	V_{IN}=1.5V	2.6	3.5	-	1.4	3.5	-	mA	③
			V_{IN}=2.0V(*2)	4.9	6.0	-	3.0	6.0	-		
			V_{IN}=3.0V(*3)	9.2	10.3	-	5.8	10.3	-		
			V_{IN}=4.0V(*4)	12.3	13.8	-	7.7	13.8	-		
Leak Current	I_{Leak}	V_{IN}=6.0V,V_{RESETB}=6.0		-	0.01	0.1	-	0.01	1	μA	④
Cd Pin Sink Current	I_{cd}	V_{IN}=1.5V, V_{Cd}=0.7V		530	770	-	295	770	-		
Release Delay Time1(*5)	t_{DR1}	V_{IN}=1.5V→$V_{DF(T)}$×1.1, Cd=0.01μF		8.5	10.0	11.5	7	10.0	12	ms	⑤
Release Delay Time2(*6)	t_{DR2}	$V_{IN}=V_{DF(T)}$×1.1, Cd=0.01μF		0.85	1.0	1.15	0.7	1.0	1.2		
Watchdog Timeout Period(*7)	t_{WD}	$V_{IN}=V_{DF(T)}$×1.1V, Cd=0.01μF,WD=V_{SS}		8.5	10.0	11.5	7	10.0	12		
Detect Delay Time(*8)	t_{DF}	$V_{IN}=V_{DF(T)}$×1.1→1.5V, Cd=0.01μF		-	10.0	50	-	10.0	100	μs	
Watchdog Pulse Width	t_{WDIN}	V_{IN}=6.0V, Cd=0.01μF Apply pulse from 6.0V to 0V to the WD pin.		100	-	-	100	-	-	ns	⑥
Watchdog High Level Voltage	V_{WDH}	$V_{IN}=V_{DF(T)}$×1.1→6.0V		V_{IN}×0.7	-	6	V_{IN}×0.7	-	6	V	
Watchdog Low Level Voltage	V_{WDL}	$V_{IN}=V_{DF(T)}$×1.1→6.0V		0	-	V_{IN}×0.3	0	-	V_{IN}×0.3	V	
Watchdog Pull-down Resistance	R_{WD}	V_{WD}=6.0V, $R_{WD}=V_{WD}/I_{WD}$		280	550	1100	220	550	1350	kΩ	⑦
MRB High Level Voltage	V_{MRH}	$V_{IN}=V_{DF(T)}$×1.1~6.0V		1.3	-	V_{IN}	1.3	-	V_{IN}	V	⑧
MRB Low Level Voltage	V_{MRL}			0	-	0.45	0	-	0.45	V	
MRB Pull-up Resistance	R_{MR}	V_{IN}=6.0V, V_{MRB}=0V, $R_{MR}=V_{IN}/I_{MRB}$		300	800	1200	230	800	1420	kΩ	⑨
MRB Pulse Width	t_{MRIN}	V_{IN}=6.0V, Apply pulse from 6.0V to 0V to the MRB pin.		1.0	-	-	1.0	-	-	μs	⑩

NOTE:

*The WD pin and MRB pin are open unless otherwise specified in the measurement conditions.

(*1) $V_{DF(T)}$: Nominal detect voltage

(*2) For $V_{DF(T)}$＞2.0V products only.

(*3) For $V_{DF(T)}$＞3.0V products only.

(*4) For $V_{DF(T)}$＞4.0V products only.

(*5) Until time when RESETB pin shows release status after V_{IN} reached the release voltage.
Release voltage (V_{DR}) = Detect voltage (V_{DFL}) + Hysteresis width (V_{HYS})

(*6) The time to change the status of RESETB pin from the detect-status after the watchdog-timeout happens with the condition of WD=V_{SS}.

(*7) The time to change the status of RESETB pin from the release-status to the detect-status with the condition of WD=V_{SS}.

(*8) When V_{IN} is changed during watchdog timeout time, until time when RESETB pin shows detect status after V_{IN} reached the detect voltage.

(*9) The ambient temperature range (-40℃≦Ta≦125℃) is design Value.

■ELECTRICAL CHARACTERISTICS (Continued)

XD6131A Series

PARAMETER	SYMBOL	CONDITIONS		Ta=25℃			-40℃≦Ta≦125℃(*10)			UNITS	CIRCUIT
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Operating Voltage	V_{IN}			1.5	-	6.0	1.5	-	6.0	V	①
Detect Voltage	V_{DFL}	$V_{DF(T)}$(*1)=1.6~5.0V		$V_{DF(T)}$ ×0.99	$V_{DF(T)}$	$V_{DF(T)}$ ×1.01	$V_{DF(T)}$ ×0.975	$V_{DF(T)}$	$V_{DF(T)}$ ×1.025	V	
Temperature Characteristics	ΔV_{DFL}/ (ΔTopr·V_{DFL})	-40℃≦Topr≦125℃		-	±50	-	-	±50	-	ppm /℃	
Hysteresis Width	V_{HYS}			V_{DFL} ×0.04	V_{DFL} ×0.05	V_{DFL} ×0.06	V_{DFL} ×0.03	V_{DFL} ×0.05	V_{DFL} ×0.07	V	
Supply Current	Iss	V_{IN}=$V_{DF(T)}$ ×0.9		-	8.1	12.1	-	8.1	14.0	μA	②
		V_{IN}=$V_{DF(T)}$×1.1	EN=L(*2)	-	2.5	3.5	-	2.5	5.0		
			EN=H	-	9.8	12.6	-	9.8	13.6		
Output Current	I_{RBOUT}	N-ch. V_{RESETB}=0.3V	V_{IN}=1.5V	2.6	3.5	-	1.4	3.5	-	mA	③
			V_{IN}=2.0V(*2)	4.9	6.0	-	3.0	6.0	-		
			V_{IN}=3.0V(*3)	9.2	10.3	-	5.8	10.3	-		
			V_{IN}=4.0V(*4)	12.3	13.8	-	7.7	13.8	-		
Leakage Current	I_{Leak}	V_{IN}=6.0V, V_{RESETB}=6.0V		-	0.01	0.1	-	0.01		μA	④
Cd Pin Sink Current	I_{cd}	V_{IN}=1.5V, V_{Cd}=0.7V		530	770	-	295	770	-		
Release Delay Time1(*6)	t_{DR1}	V_{IN}=1.5V→$V_{DF(T)}$×1.1, Cd=0.01μF		8.5	10.0	11.5	7	10.0	12	ms	⑤
Release Delay Time2(*7)	t_{DR2}	V_{IN}=$V_{DF(T)}$×1.1, Cd=0.01μF		0.85	1.0	1.15	0.7	1.0	1.2		
Watchdog Timeout Period(*8)	t_{WD}	V_{IN}=$V_{DF(T)}$×1.1, Cd=0.01μF, WD=V_{SS}		8.5	10.0	11.5	7	10.0	12		
Detect Delay Time(*9)	t_{DF}	V_{IN}=$V_{DF(T)}$×1.1→1.5V, Cd=0.01μF		-	10.0	50	-	10.0	100	μs	
Watchdog Pulse Width	t_{WDIN}	V_{IN}=6.0V, Cd=0.01μF Apply pulse from 6.0V to 0V to the WD pin.		100	-	-	100	-	-	ns	⑥
Watchdog High Level Voltage	V_{WDH}	$V_{DF(T)}$×1.1≦V_{IN}≦6.0V		V_{IN}×0.7	-	6	V_{IN}×0.7	-	6	V	
Watchdog Low Level Voltage	V_{WDL}	$V_{DF(T)}$×1.1≦V_{IN}≦6.0V		0	-	V_{IN}×0.3	0	-	V_{IN}×0.3	V	
Watchdog Pull-down Resistance	R_{WD}	V_{WD}=6.0V, R_{WD}=V_{WD}/I_{WD}		280	550	1100	220	550	1350	kΩ	⑦
EN High Level Voltage	V_{ENH}	V_{IN}=$V_{DF(T)}$×1.1~6.0V		1.3	-	V_{IN}	1.3	-	V_{IN}	V	⑧
EN Low Level Voltage	V_{ENL}			0	-	0.45	0	-	0.45	V	⑨
EN Pull-up Resistance	R_{EN}	V_{IN}=6.0V,V_{EN}=0V, R_{EN}=V_{IN}/I_{EN}		300	800	1200	230	800	1420	kΩ	

NOTE:

* The WD pin and EN pin are open unless otherwise specified in the measurement conditions.

(*1) $V_{DF(T)}$: Nominal detect voltage

(*2) Excludes the current that flows to EN pull-up resistance when EN = L.

(*3) For $V_{DF(T)}$＞2.0V products only.

(*4) For $V_{DF(T)}$＞3.0V products only.

(*5) For $V_{DF(T)}$＞4.0V products only.

(*6) Until time when RESETB pin shows release status after V_{IN} reached the release voltage.
Release voltage (V_{DR}) = Detect voltage (V_{DFL}) + Hysteresis width (V_{HYS})

(*7) The time to change the status of RESETB pin from the detect-status after the watchdog-timeout happens with the condition of WD=V_{SS}.

(*8) The time to change the status of RESETB pin from the release-status to the detect-status with the condition of WD=V_{SS}.

(*9) When V_{IN} is changed during watchdog timeout time, until time when RESETB pin shows detect status after V_{IN} reached the detect voltage.

(*10) The ambient temperature range (-40℃≦Ta≦125℃) is design Value.

■ELECTRICAL CHARACTERISTICS (Continued)

XD6131B Series

PARAMETER	SYMBOL	CONDITIONS		Ta=25℃			-40℃≦Ta≦125℃(*10)			UNITS	CIRCUIT
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Operating Voltage	V_{IN}			1.5	-	6.0	1.5	-	6.0	V	①
Detect Voltage	V_{DFL}	$V_{DF(T)}$(*1)=1.6~5.0V		$V_{DF(T)}$ ×0.99	$V_{DF(T)}$	$V_{DF(T)}$ ×1.01	$V_{DF(T)}$ ×0.975	$V_{DF(T)}$	$V_{DF(T)}$ ×1.025	V	
Temperature Characteristics	$\Delta V_{DFL}/(\Delta Topr \cdot V_{DFL})$	-40℃≦Topr≦125℃		-	±50	-	-	±50	-	ppm /℃	
Hysteresis Width	V_{HYS}			V_{DFL} ×0.04	V_{DFL} ×0.05	V_{DFL} ×0.06	V_{DFL} ×0.03	V_{DFL} ×0.05	V_{DFL} ×0.07	V	
Supply Current	Iss	$V_{IN}=V_{DF(T)}$ ×0.9		-	8.1	12.1	-	8.1	14.0	μA	②
		$V_{IN}=V_{DF(T)}$×1.1	ENB=H(*2)	-	2.5	3.5	-	2.5	5.0		
			ENB=L	-	9.8	12.6	-	9.8	13.6		
Output Current	I_{RBOUT}	N-ch. V_{RESETB}=0.3V	V_{IN}=1.5V	2.6	3.5	-	1.4	3.5	-	mA	③
			V_{IN}=2.0V(*2)	4.9	6.0	-	3.0	6.0	-		
			V_{IN}=3.0V(*3)	9.2	10.3	-	5.8	10.3	-		
			V_{IN}=4.0V(*4)	12.3	13.8	-	7.7	13.8	-		
Leakage Current	I_{Leak}	V_{IN}=6.0V, V_{RESETB}=6.0V		-	0.01	0.1	-	0.01		μA	④
Cd Pin Sink Current	I_{cd}	V_{IN}=1.5V, V_{Cd}=0.7V		530	770	-	295	770	-		
Release Delay Time1(*6)	t_{DR1}	V_{IN}=1.5V→$V_{DF(T)}$×1.1, Cd=0.01μF		8.5	10.0	11.5	7	10.0	12	ms	⑤
Release Delay Time2(*7)	t_{DR2}	$V_{IN}=V_{DF(T)}$×1.1, Cd=0.01μF		0.85	1.0	1.15	0.7	1.0	1.2		
Watchdog Timeout Period(*8)	t_{WD}	$V_{IN}=V_{DF(T)}$×1.1, Cd=0.01μF, WD=V_{SS}		8.5	10.0	11.5	7	10.0	12		
Detect Delay Time(*9)	t_{DF}	$V_{IN}=V_{DF(T)}$×1.1→1.5V, Cd=0.01μF		-	10.0	50	-	10.0	100	μs	
Watchdog Pulse Width	t_{WDIN}	V_{IN}=6.0V, Cd=0.01μF Apply pulse from 6.0V to 0V to the WD pin.		100	-	-	100	-	-	ns	⑥
Watchdog High Level Voltage	V_{WDH}	$V_{DF(T)}$ × 1.1≦V_{IN}≦6.0V		V_{IN}×0.7	-	6	V_{IN}×0.7	-	6	V	
Watchdog Low Level Voltage	V_{WDL}	$V_{DF(T)}$ × 1.1≦V_{IN}≦6.0V		0	-	V_{IN}×0.3	0	-	V_{IN}×0.3	V	
Watchdog Pull-down Resistance	R_{WD}	V_{WD}=6.0V, $R_{WD}=V_{WD}/I_{WD}$		280	550	1100	220	550	1350	kΩ	⑦
ENB High Level Voltage	V_{ENBH}	$V_{IN}=V_{DF(T)}$×1.1~6.0V		1.3	-	V_{IN}	1.3	-	V_{IN}	V	⑧
ENB Low Level Voltage	V_{ENBL}			0	-	0.45	0	-	0.45	V	⑨
ENB Pull-down Resistance	R_{ENB}	V_{ENB}=6.0V, $R_{ENB}=V_{ENB}/I_{ENB}$		300	800	1200	230	800	1420	kΩ	

NOTE:

*The WD pin and ENB pin are open unless otherwise specified in the measurement conditions.

(*1) $V_{DF(T)}$: Nominal detect voltage

(*2) Excludes the current that flows to the EN pull-down resistance when ENB = H.

(*3) For $V_{DF(T)}$ > 2.0V products only.

(*4) For $V_{DF(T)}$ > 3.0V products only.

(*5) For $V_{DF(T)}$ > 4.0V products only.

(*6) Until time when RESETB pin shows release status after V_{IN} reached the release voltage.
Release voltage (V_{DR}) = Detect voltage (V_{DFL}) + Hysteresis width (V_{HYS})

(*7) The time to change the status of RESETB pin from the detect-status after the watchdog-timeout happens with the condition of WD=V_{SS}.

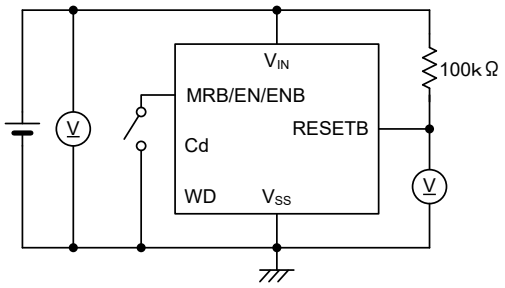
(*8) The time to change the status of RESETB pin from the release-status to the detect-status with the condition of WD=V_{SS}.

(*9) When V_{IN} is changed during watchdog timeout time, until time when RESETB pin shows detect status after V_{IN} reached the detect voltage.

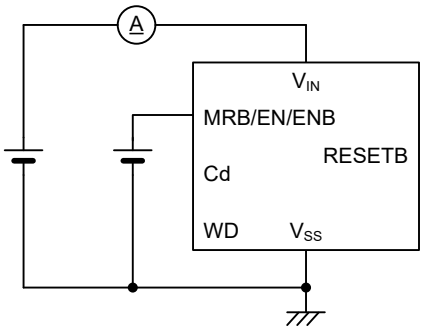
(*10) The ambient temperature range (-40℃≦Ta≦125℃) is design Value.

■ TEST CIRCUITS

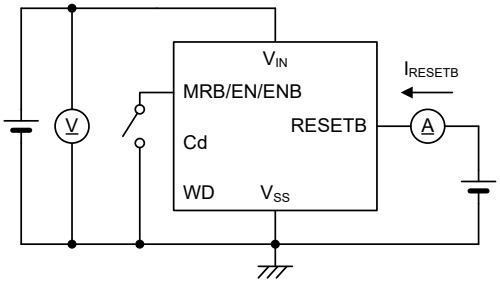
CIRCUIT①



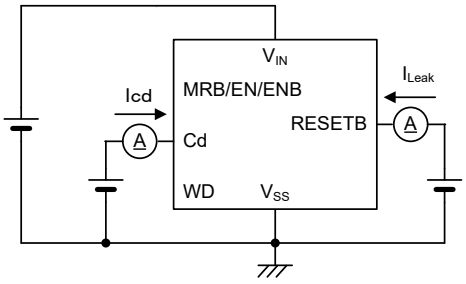
CIRCUIT②



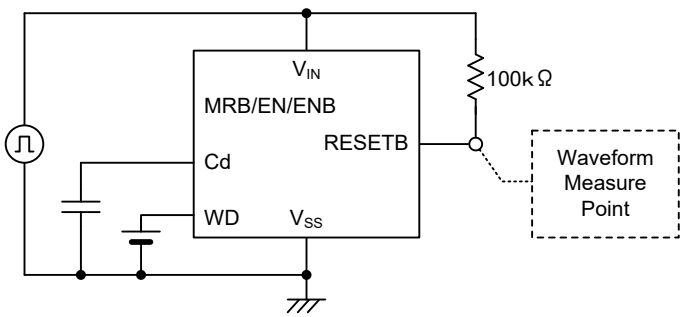
CIRCUIT③



CIRCUIT④

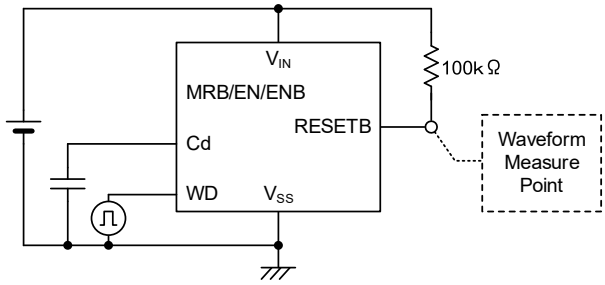


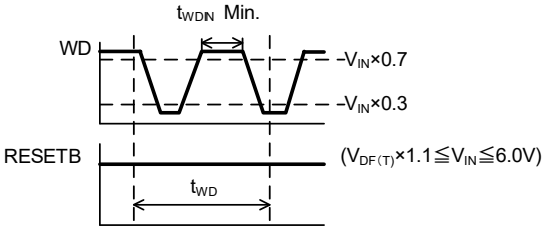
CIRCUIT⑤



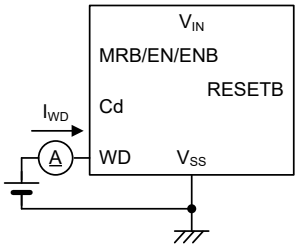
■ TEST CIRCUITS (Continued)

CIRCUIT⑥

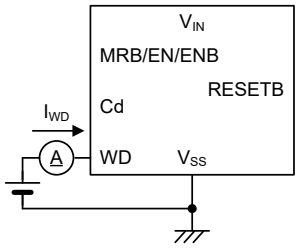




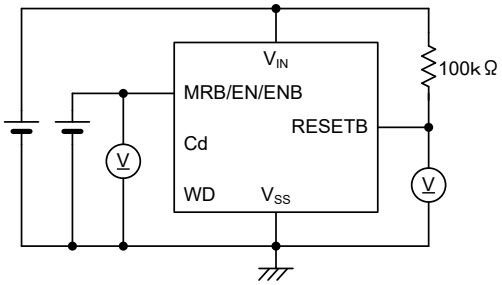
CIRCUIT⑦



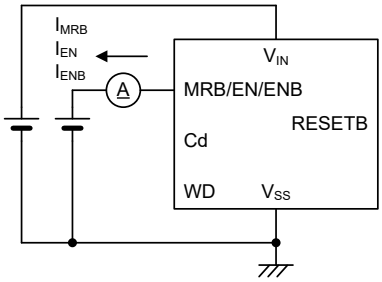
CIRCUIT⑦



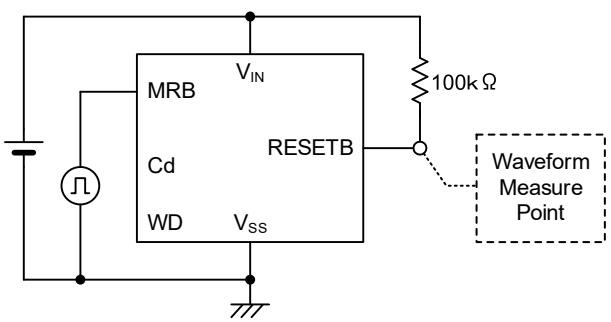
CIRCUIT⑧

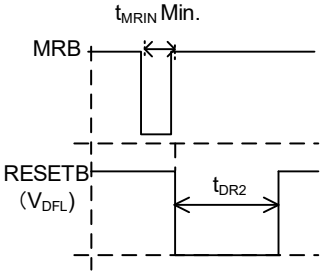


CIRCUIT⑨



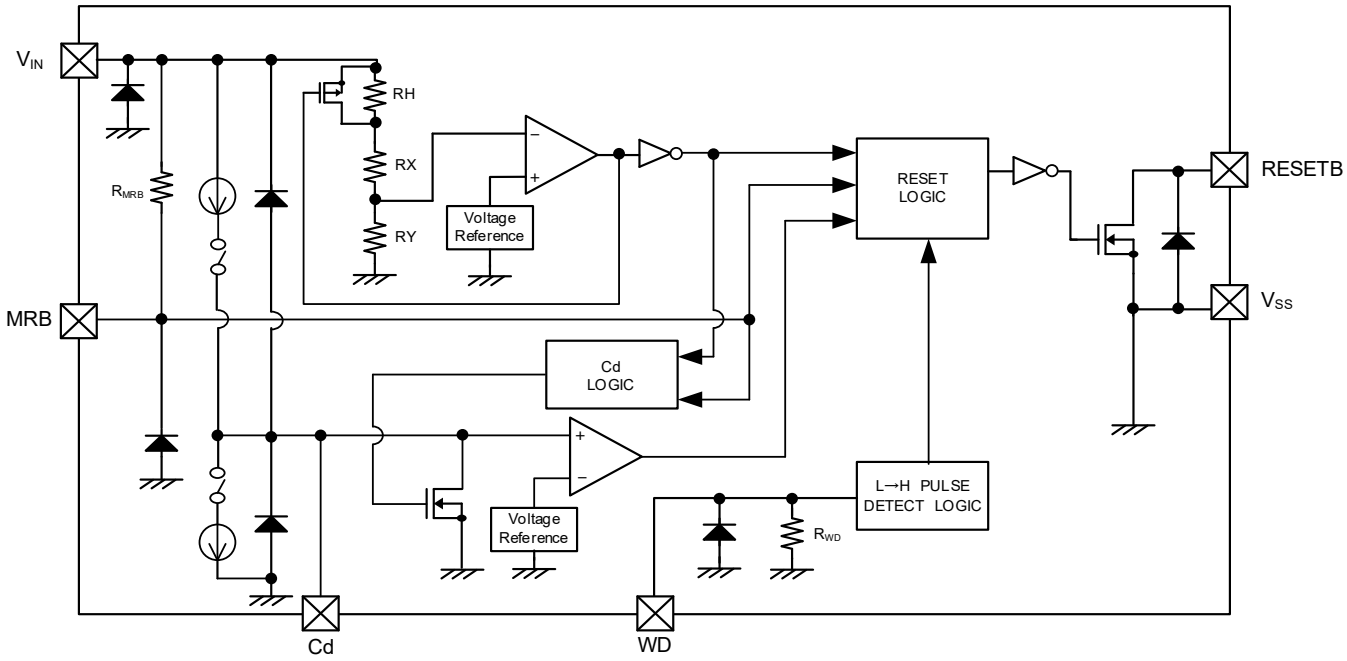
CIRCUIT⑩





■OPERATIONAL EXPLANATION

In the XD6130/XD6131 Series, the voltage divided by RH, RX, and RY connected to the V_{IN} pin is compared to the internal reference voltage by the comparator, and the resulting output signal drives the watchdog logic and output driver. The V_{IN} pin voltage is gradually lowered, and when the V_{IN} pin voltage reaches the detect voltage, H→L level signal is output to the reset output pin (V_{DFL} type).



XD6130 Series

<Output signal of reset output pin>

If the V_{IN} pin voltage is below the detect voltage, the reset output pin outputs H→L level signal.
After the V_{IN} pin voltage reaches the release voltage, the reset output pin holds L level during release delay time1 (t_{DR1}). If a start signal is not input to the WD pin within the watchdog timeout time, the reset output pin holds L level during release delay time 2 (t_{DR2}) and then outputs H level signal.

<Hysteresis>

If the internal comparator outputs L level signal, the PMOS transistor connected in parallel to RH turns ON and the hysteresis circuit activates. The hysteresis voltage width is obtained from the difference between the detect voltage and the release voltage.
The hysteresis width is V_{DFL}×0.05 (TYP.).

<WD pin>

A watchdog timer is used to detect abnormal operation and runaway in a microprocessor. If “L→H” signal is not input from the microprocessor within the watchdog timeout time, the reset output pin holds the detect state during release delay time 2 (t_{DR2}), and then L→H level signal is output to the reset output pin.
In addition, the watchdog pin is pulled down internally to V_{SS}, and when the watchdog pin is OPEN, a reset signal is output after the watchdog timeout time.

The watchdog timeout time (t_{WD}) can be set using the equation below.

t_{WD}＝Cd×10^6
Example: When Cd is 0.1μF, t_{WD}=0.1×10^{-6}×10^6 = 100ms (TYP.)

■OPERATIONAL EXPLANATION (Continued)

<Release delay time 1>

When power is added on the V_{IN}, the time from the point that V_{IN} reaches the release voltage until the reset output pin reaches the release voltage is release delay time 1 (t_{DR1}).

Release delay time 1 (t_{DR1}) can be set using the equation below.

$t_{DR1}=Cd\times10^{6}$

Example: When Cd is 0.1μF, $t_{DR1}= 0.1\times10^{-6}\times10^{6}=100ms$ (TYP.)

<Release delay time 2>

Release delay time 2 (t_{DR2}) is the duration of the detect state until the watchdog timer restarts when "L → H" signal is not input to the WD pin within the watchdog timeout time.

Release delay time 2 (t_{DR2}) can be set using the equation below.

$t_{DR2}=Cd\times10^{5}$

Example: When Cd is 0.1μF, $t_{DR2}=0.1\times10^{-6}\times10^{5}=10ms$ (TYP.)

<Detect delay time>

The detect delay time (t_{DF}) is the time until the V_{IN} pin voltage drops to the detect voltage and the reset output pin enters the detect state.

<MRB pin> *XD6130 Series

The MRB pin voltage can be input to force the signal of the reset output pin to the detect state.

When the MRB pin voltage input reaches an H→L level signal, an H→L level signal is output to the reset output pin. After the MRB pin voltage reaches L→H level, the reset output pin holds the detect state during release delay time 1(t_{DR1}).

<EN pin> *XD6131A Series

If the watchdog function will not be used, the EN pin can be set to L level to forcibly stop only the watchdog function and keep the voltage detector operating. When using the watchdog function, use the EN pin at H level. If the input voltage and EN pin voltage reach L→H level, the reset output pin holds the detect state during release delay time 1 (t_{DR1}). (Refer to Timing Chart 2, ①)

If the input voltage is higher than the release voltage and the EN pin voltage reaches L→H level, the watchdog function recovers. (Refer to Timing Chart 2, ②)

<ENB Pin> *XD6131B Series

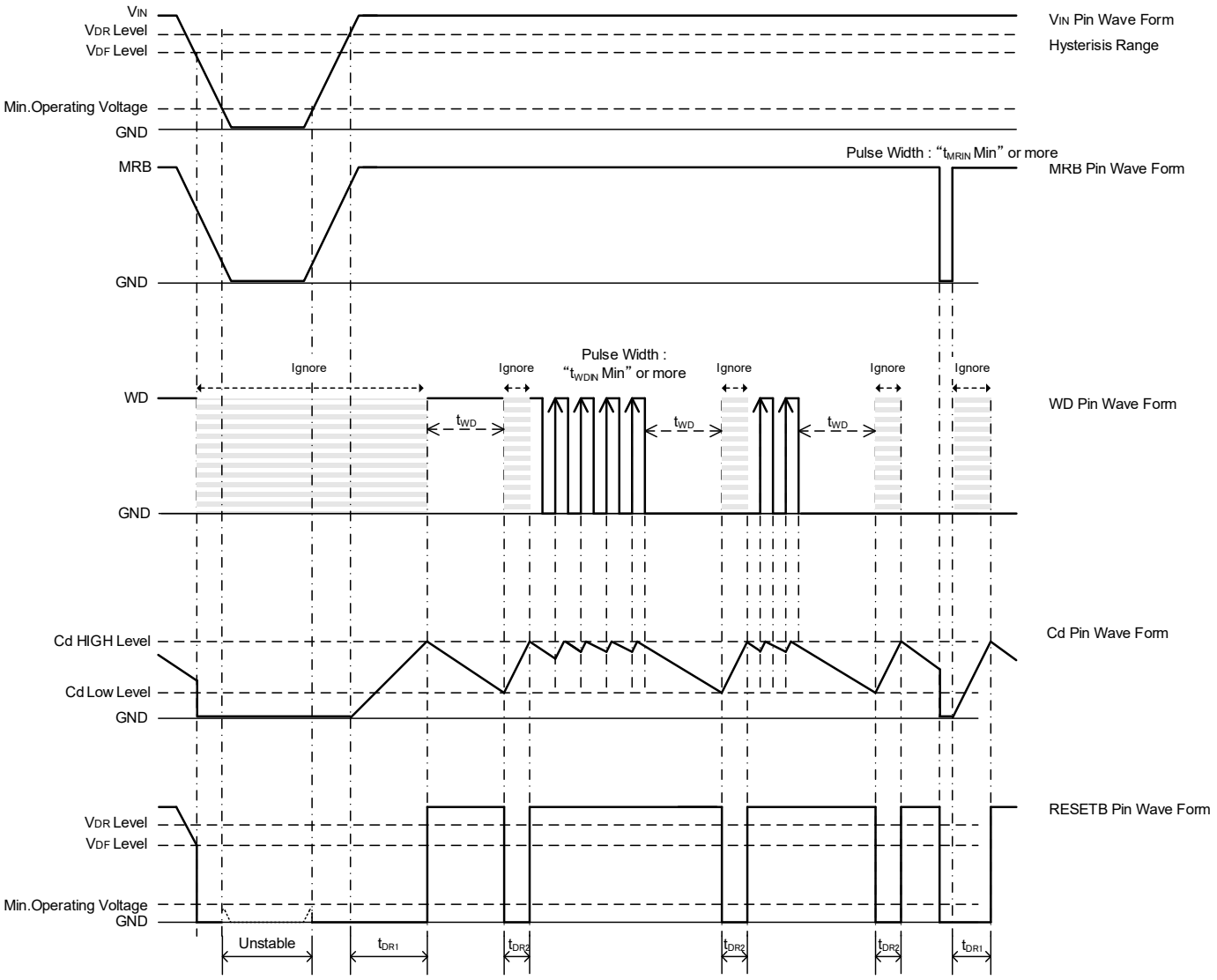
When the watchdog function is not used, the ENB pin can be set to H level to keep the voltage detector operating and forcibly stop only the watchdog function. To use the watchdog function, use the ENB pin at L level. When the input voltage and ENB pin voltage reach H→L level, the reset output pin holds the detect state during release delay time 1 (t_{DR1}). (Refer to Timing Chart 3, ①)

When the input voltage is higher than the release voltage and the ENB pin voltage reaches H→L level, the watchdog function recovers. (Refer to Timing Chart 3, ②)

■OPERATIONAL EXPLANATION (Continued)

<Timing Chart 1>

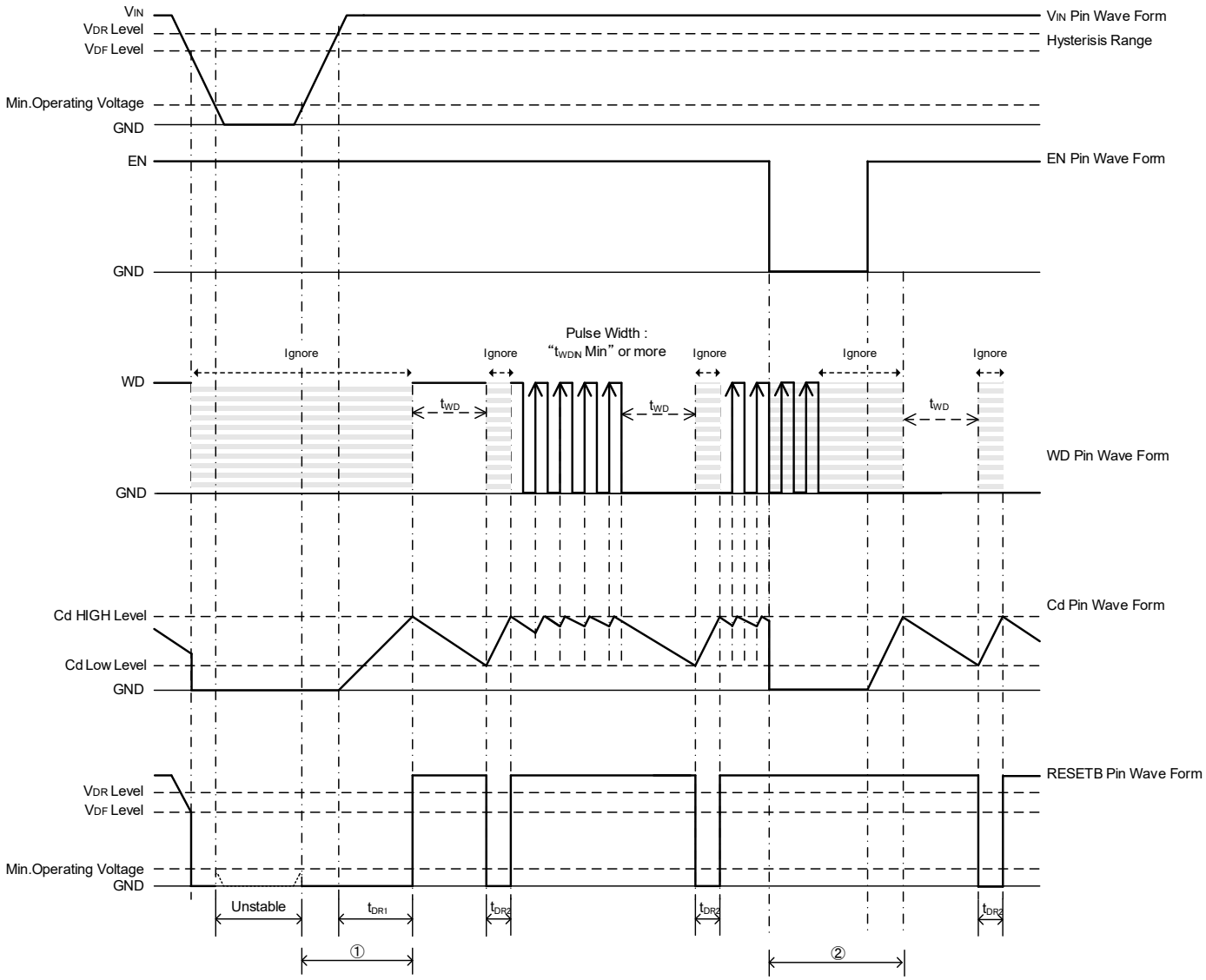
XD6130 Series



■OPERATIONAL EXPLANATION (Continued)

<Timing Chart 2>

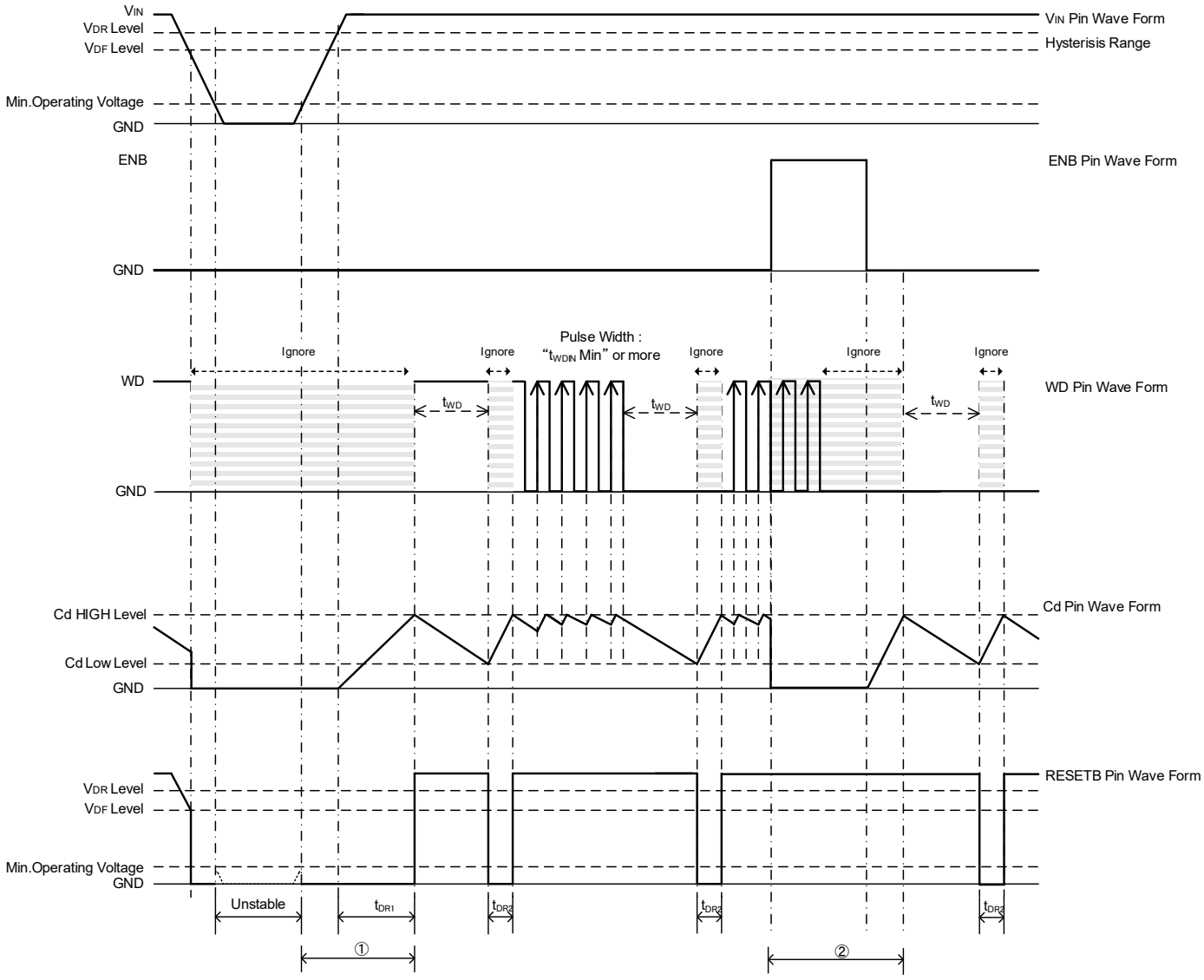
XD6131A Series



■OPERATIONAL EXPLANATION(Continued)

<Timing Chart 3>

XD6131B Series



■NOTES ON USE

1. Use this IC within the absolute maximum ratings. Risk of deterioration or damage if the absolute maximum ratings are exceeded during temporary or transient voltage drops or voltage jumps.

2. If a resistance is added between the power and the VIN pin, the flowthrough current when the IC operates will cause the V_{IN} pin voltage to drop and the IC may malfunction.

3. When raising the input voltage from the minimum operating voltage or less, if changed suddenly, the release delay time may become short.

4. Sufficiently reinforce the V_{IN} and GND lines, as power noise may cause malfunctioning of the watchdog function and voltage detector. It is recommended that a capacitor be added between V_{IN} and GND.

5. Enter “H” level, or “L” level should be fed to MRB and EN/ENB pin.

6. To ensure stable operation of the watchdog function, be sure to add a capacitor at the Cd pin.
   The release delay time and watchdog timeout time are affected by the accuracy and temperature characteristics of the Cd pin capacitor.

7. If the Cd pin capacitor is unable to discharge to the ground level during recovery after a power interruption, the release delay may become noticeably shorter. Exercise caution.

8. The output voltage at detection is determined by the pull-up resistance connected to RESETB pin.
   Select the resistance based on the following considerations:

   At detection: $V_{RESETB}=(Vpull\text{-}Up)/(1+Rpull/R_{ON})$
   Vpull-Up: Voltage after pull-up
   R_{ON} (*1): ON resistance of N-ch driver (calculated from V_{RESETB}/I_{RBOUT1} in electrical characteristics)(*3)

   Example calculation:
   When V_{IN}=2.0V (*2), $R_{ON}=0.3/4.9\times10^{-3}\fallingdotseq61.2\Omega$(MAX.). If you wish to make the VRESETB voltage at detection 0.1V or lower with Vpull-Up=3.0V,
   $Rpull=(Vpull\text{-}Up/V_{RESETB}-1)\times R_{ON}=(3/0.1-1)\times61.2\fallingdotseq1.8k\Omega$,
   and thus to make the output voltage at detection 0.1V or less under the above conditions, the pull-up resistance must be 1.8kΩ or higher.

(*1) The smaller V_{IN} is, the larger R_{ON} becomes.
(*2) When selecting V_{IN}, calculate using the lowest value of the input voltage range you will use.
(*3) I_{RBOUT1} specified in the electrical characteristics is the value at Ta=25℃. I_{RBOUT1} varies depending on the ambient temperature.
To select the pull-up resistance taking ambient temperature into account, please calculate I_{RBOUT} with the MIN. value of the ambient temperature range of -40℃≦Ta≦125℃.

   At release: $V_{RESETB}=(Vpull\text{-}Up)/(1+Rpull/R_{OFF})$
   Vpull-Up: Voltage after pull-up
   R_{OFF}: Resistance value 60MΩ(MIN.)
   when N-ch driver is OFF (calculated from V_{RESETB}/I_{LEAK} in electrical characteristics)

   Calculation example:
   If you wish to make V_{RESETB} 5.99V or higher with Vpull-Up=6.0V
   $Rpull=(Vpull\text{-}Up/V_{RESETB}-1)\times R_{OFF}=(6/5.99-1)\times60\times10^{6}\fallingdotseq100k\Omega$,
   and thus to make the output voltage 5.99V or higher at release under the above conditions, the pull-up resistance must be 100kΩ or less.

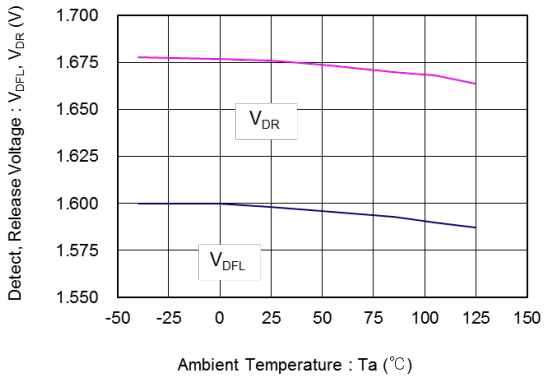
9. With the XD6131 series, the Cd pin capacitor is discharged when the watchdog function is stopped with EN or ENB.
   If the watchdog function is restarted when the Cd pin voltage is Cd Low Level (TYP. 0.25V) or higher, the L level may be output to the output pin. When restarting the watchdog function, secure a sufficient period for stopping the function and discharge the Cd pin capacitor before use.

10. We place importance on improving our products and increasing reliability. However, please design safety into the device and system, including fail-safe design and post-aging treatment.

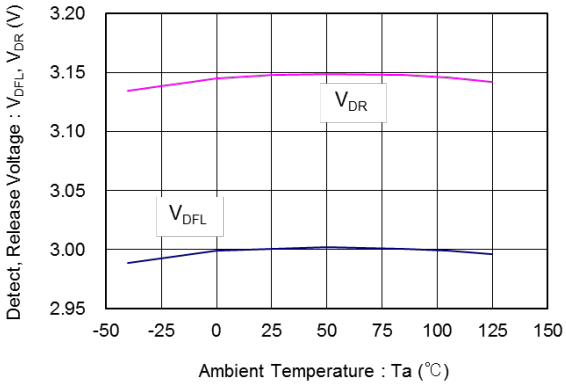
■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Detect, Release Voltage vs. Ambient Temperature

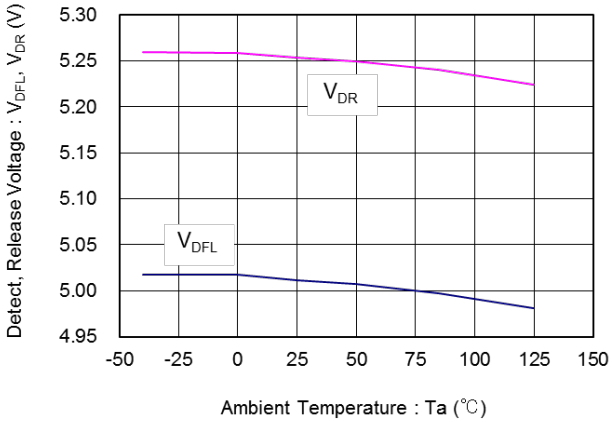
XD6130,XD6131 ($V_{DF(T)}$=1.6V)



XD6130,XD6131 ($V_{DF(T)}$=3.0V)

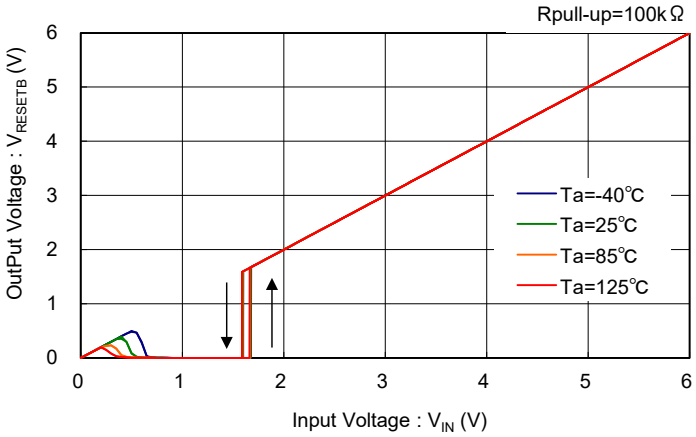


XD6130,XD6131 ($V_{DF(T)}$=5.0V)

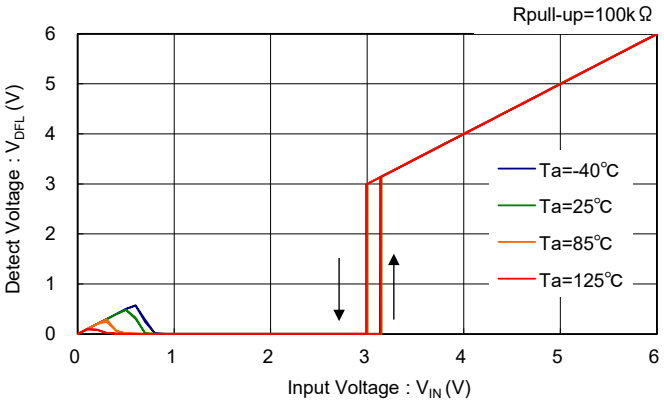


(2) Detect, Release Voltage vs. Input Voltage

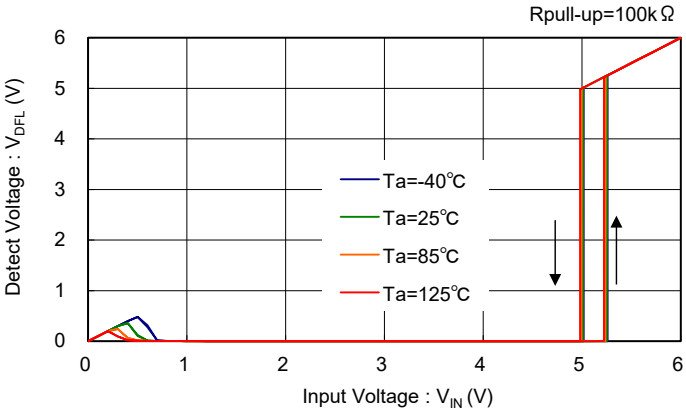
XD6130,XD6131 ($V_{DF(T)}$=1.6V)



XD6130,XD6131 ($V_{DF(T)}$=3.0V)



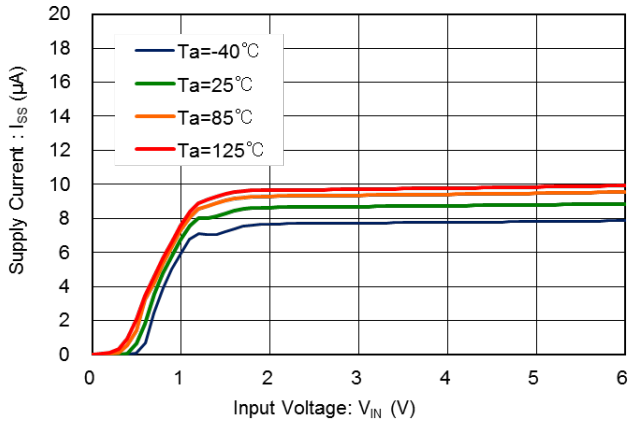
XD6130,XD6131 ($V_{DF(T)}$=5.0V)



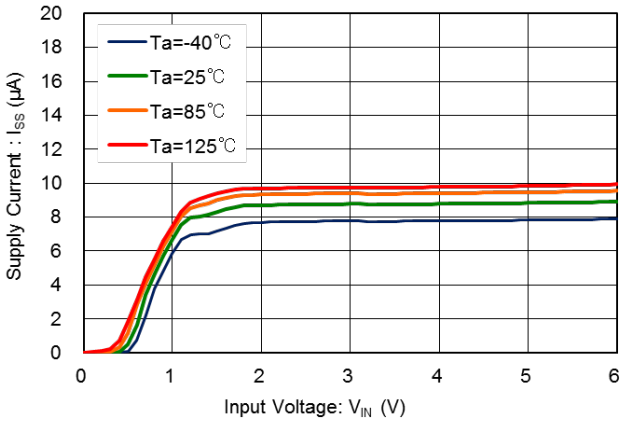
■TYPICAL PERFORMANCE CHARACTERISTICS

(3) Supply Current vs. Input Voltage

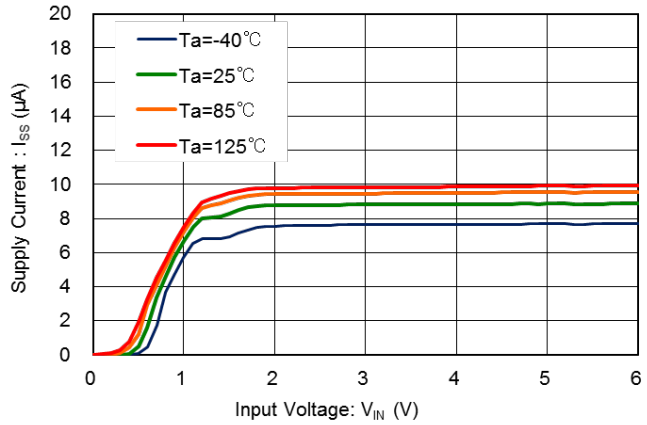
XD6130 ($V_{DF(T)}$=1.6V)



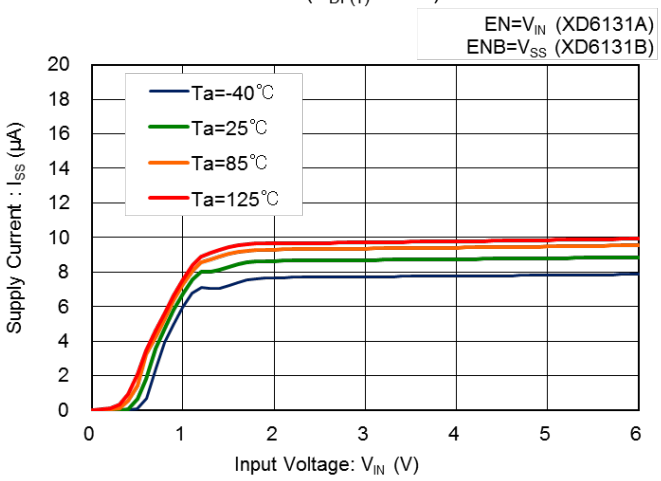
XD6130 ($V_{DF(T)}$=3.0V)



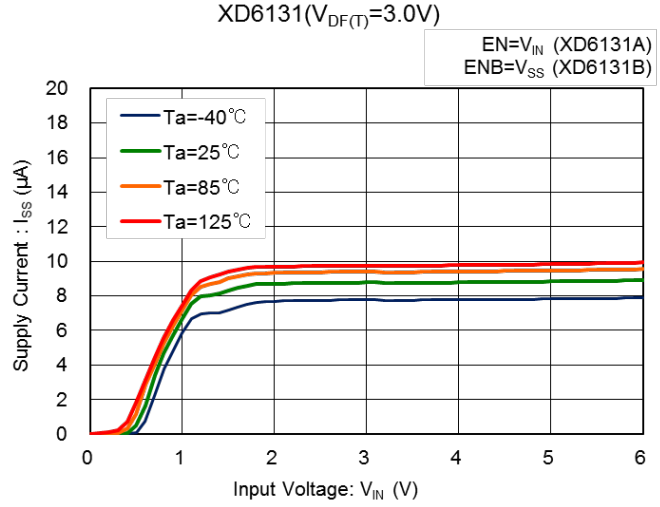
XD6130 ($V_{DF(T)}$=5.0V)



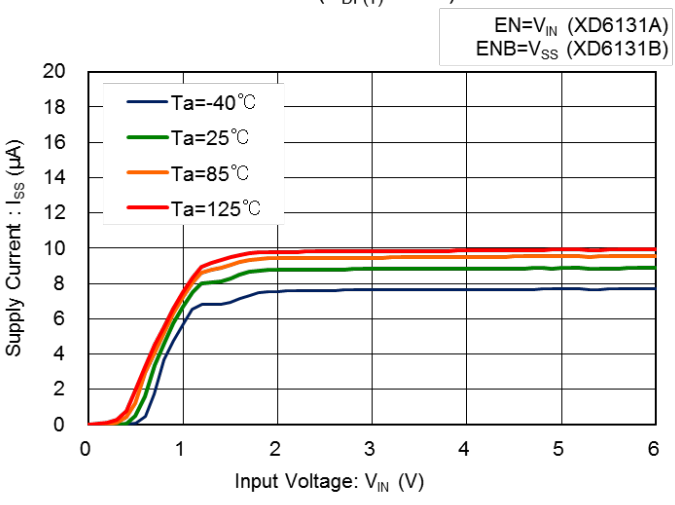
XD6131 ($V_{DF(T)}$=1.6V)



XD6131($V_{DF(T)}$=3.0V)



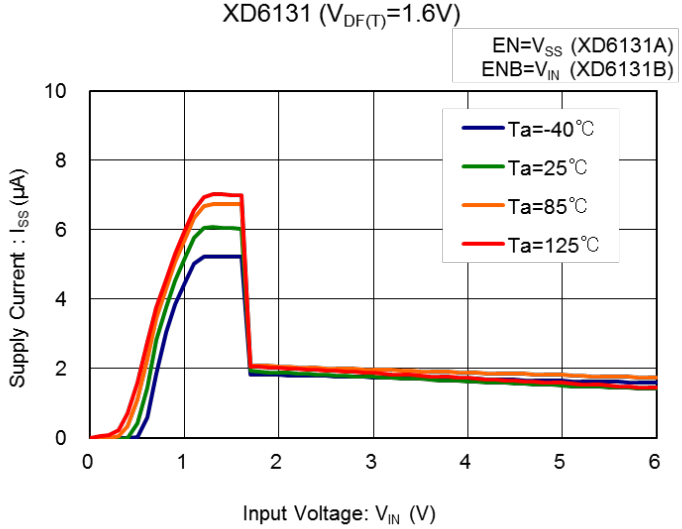
XD6131 ($V_{DF(T)}$=5.0V)



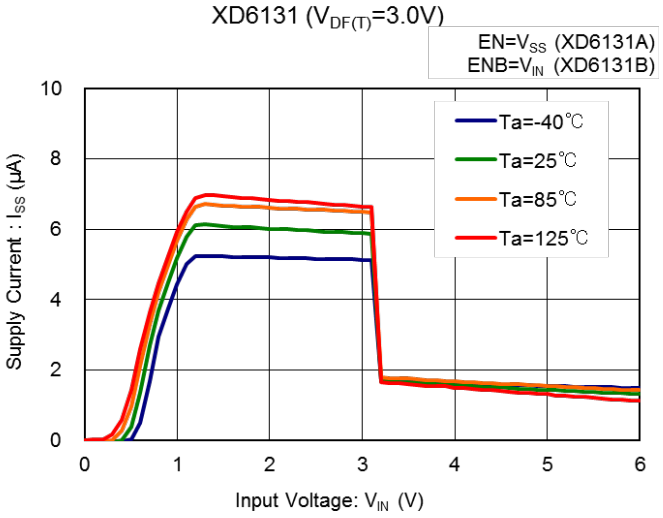
■TYPICAL PERFORMANCE CHARACTERISTICS

(3) Supply Current vs. Input Voltage (Continued)

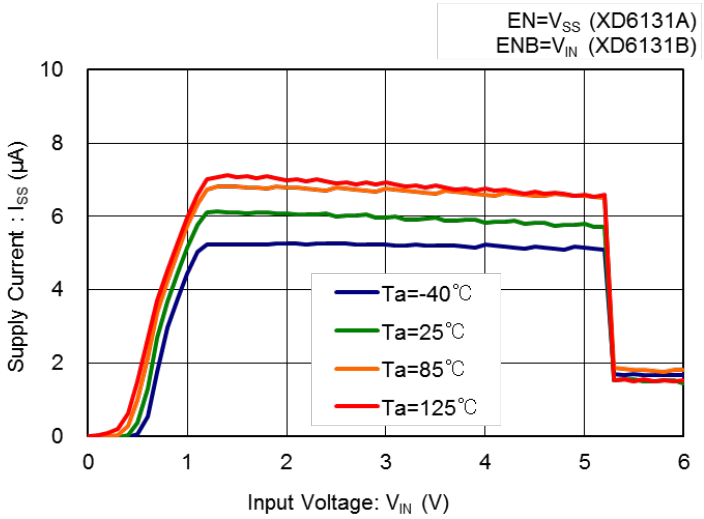
XD6131 ($V_{DF(T)}$=1.6V)



XD6131 ($V_{DF(T)}$=3.0V)

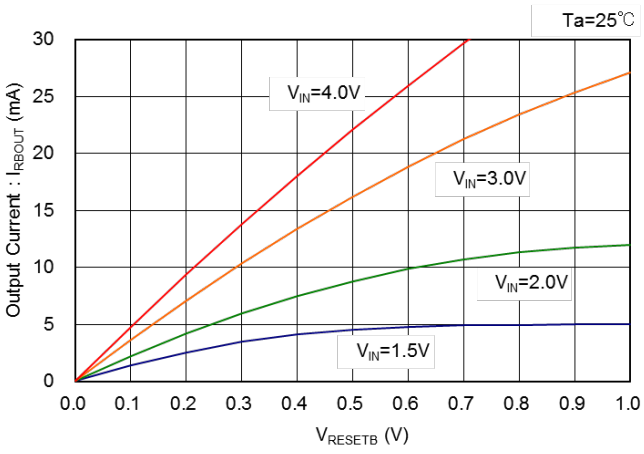


XD6131 ($V_{DF(T)}$=5.0V)



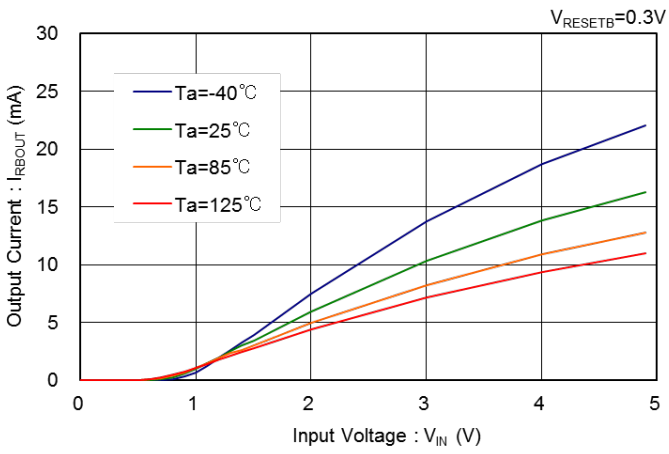
(4) Output Current vs. V_{RESETB}

XD6130,XD6131



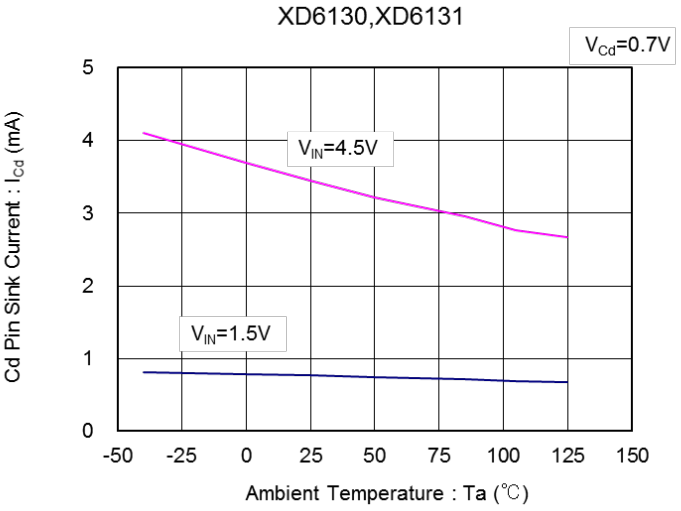
(5) Output Current vs. Input Voltage

XC6130,XC6131

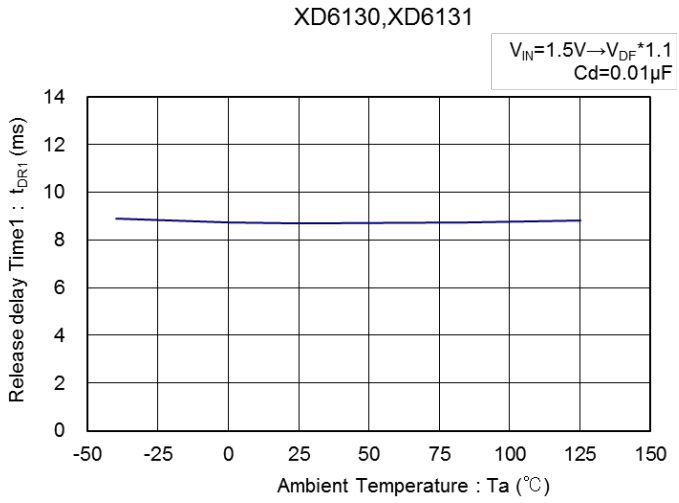


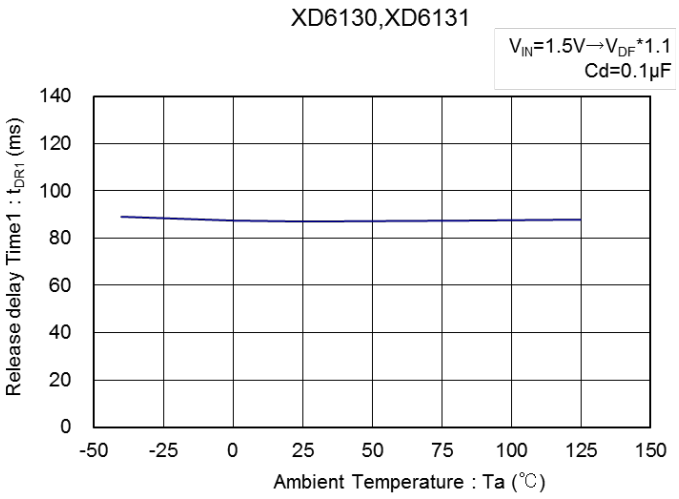
■TYPICAL PERFORMANCE CHARACTERISTICS

(6) Cd Sink Current vs. Ambient Temperature

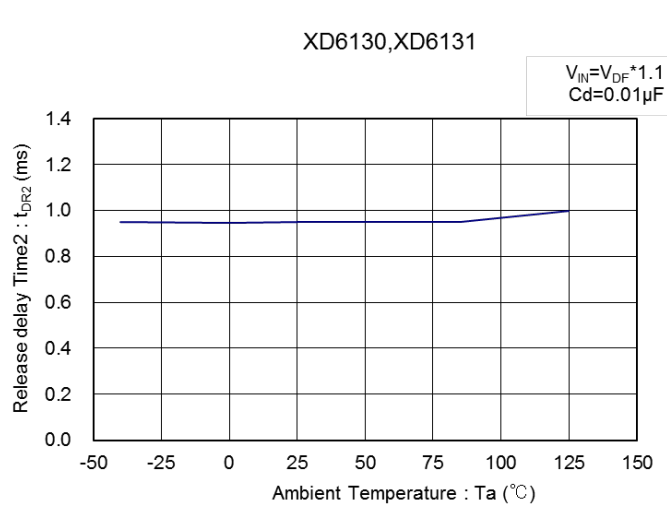


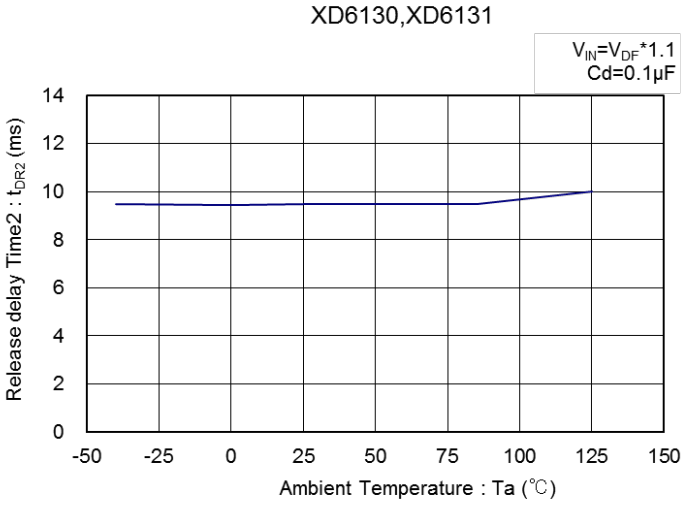
(7) Release Delay Time1 vs. Ambient Temperature





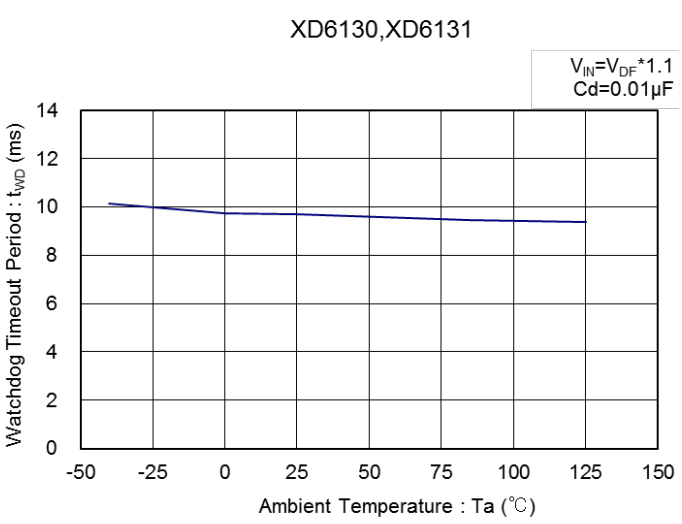
(8) Release Delay Time2 vs. Ambient Temperature

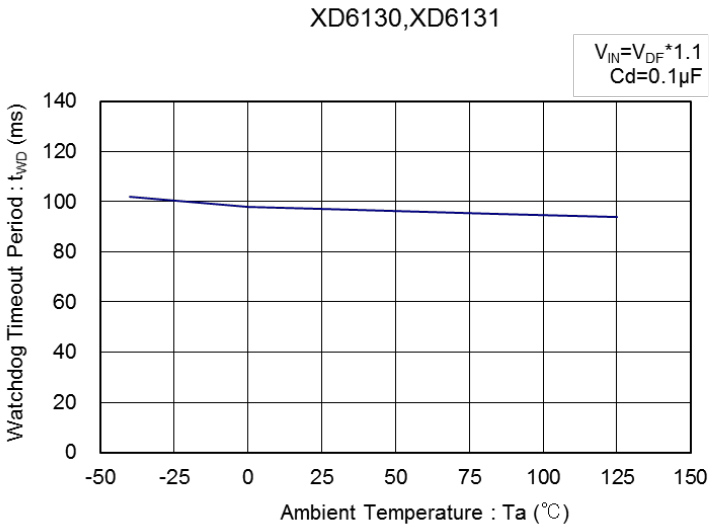




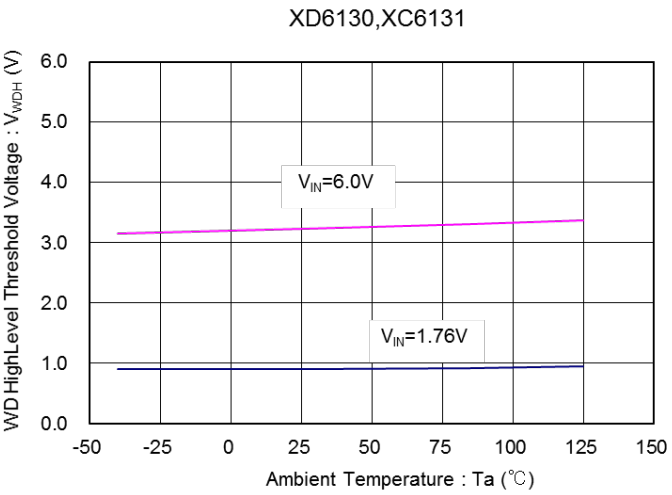
■TYPICAL PERFORMANCE CHARACTERISTICS

(9) Watchdog Timeout Period vs. Ambient Temperature

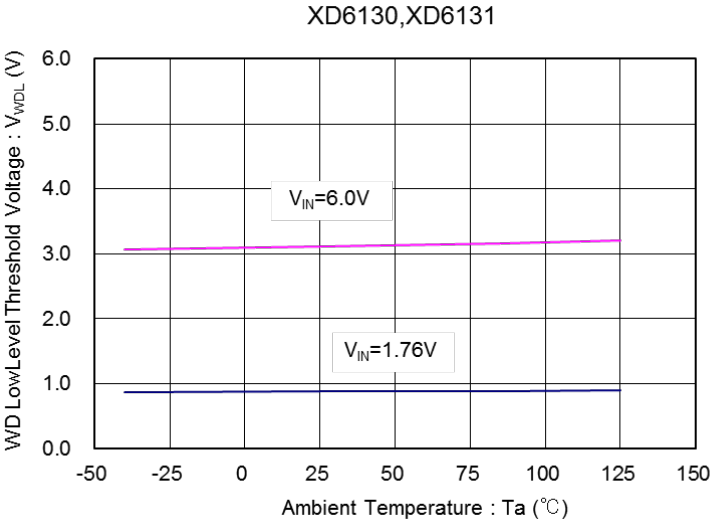


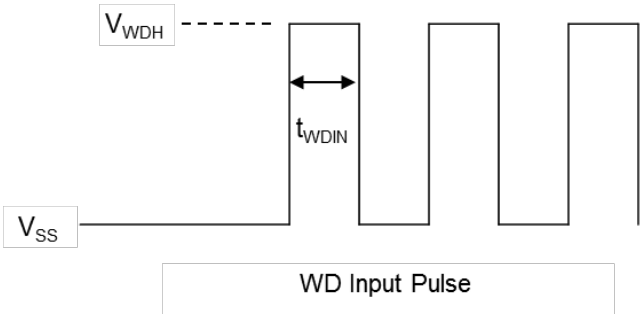


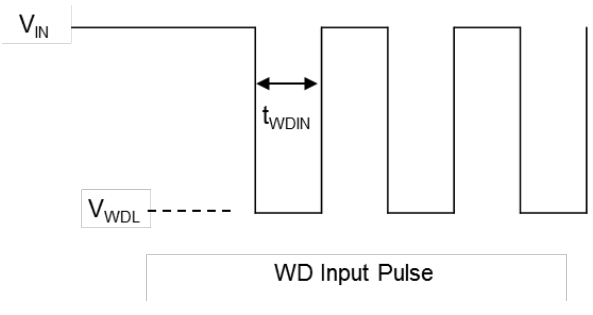
(10) WD High Level Threshold Voltage vs. Ambient Temperature



(11) WD Low Level Threshold Voltage vs. Ambient Temperature

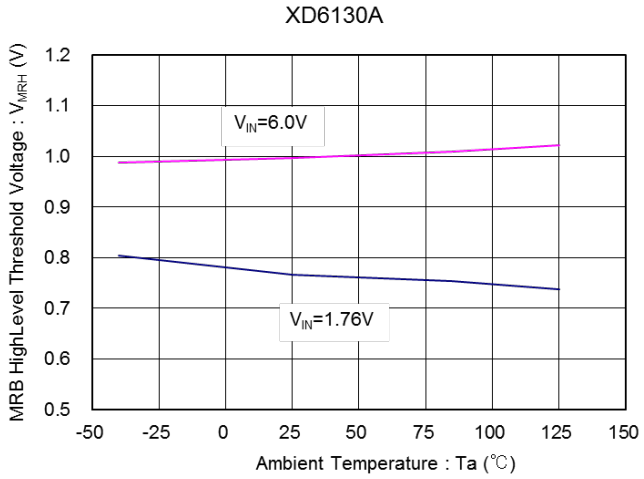




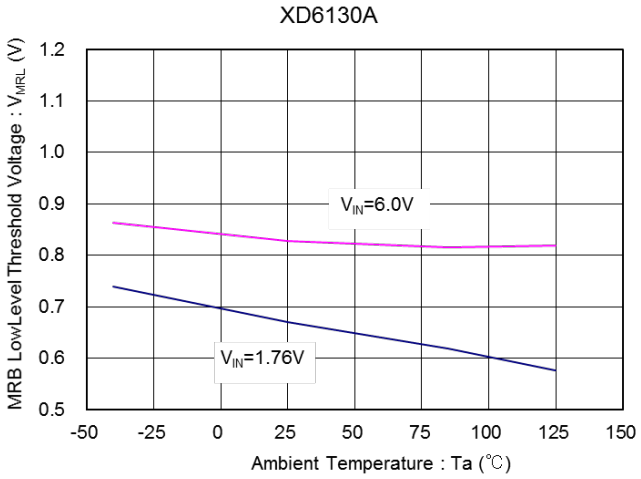


■TYPICAL PERFORMANCE CHARACTERISTICS

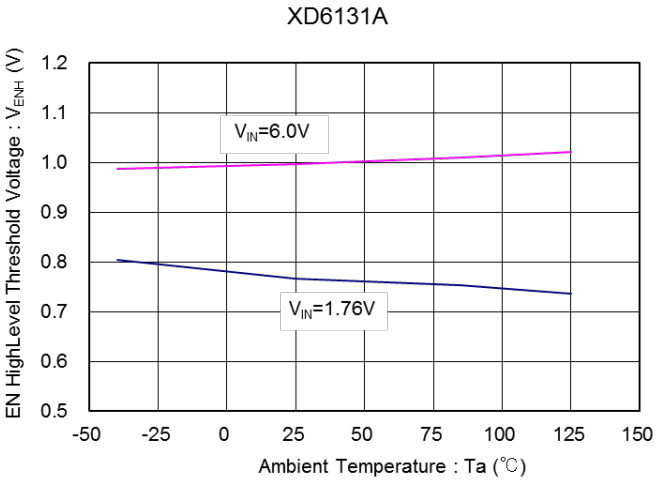
(12) MRB High Level Threshold Voltage vs. Ambient Temperature



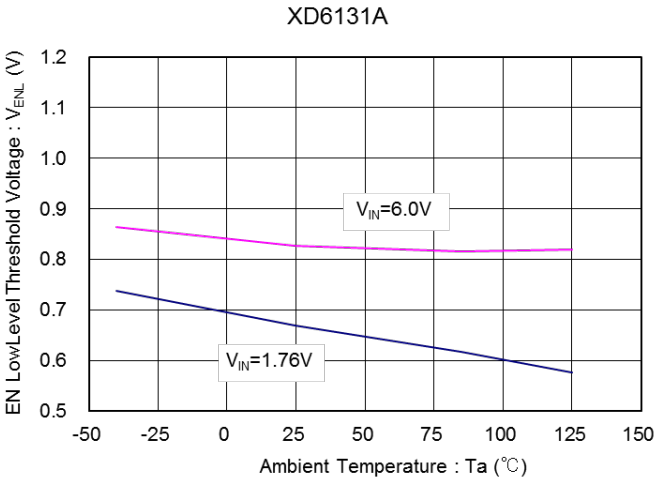
(13) MRB Low Level Threshold Voltage vs. Ambient Temperature



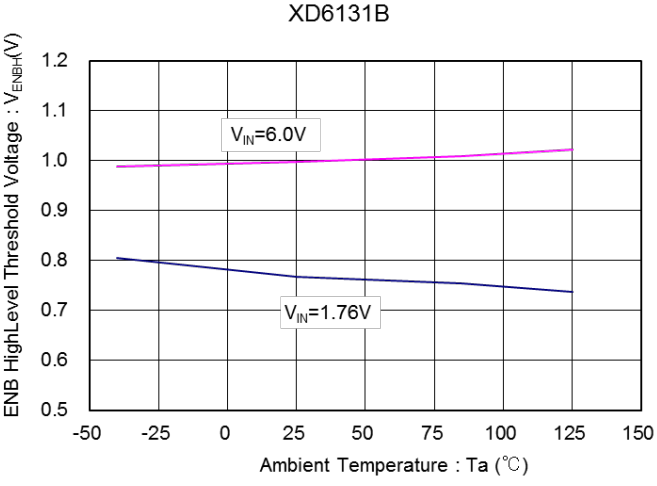
(14) EN High Level Threshold Voltage vs. Ambient Temperature



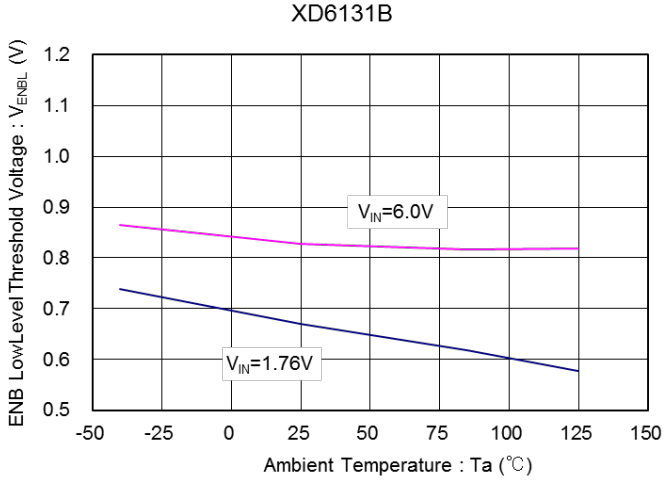
(15) EN Low Level Threshold Voltage vs. Ambient Temperature



(16) ENB High Level Threshold Voltage vs. Ambient Temperature

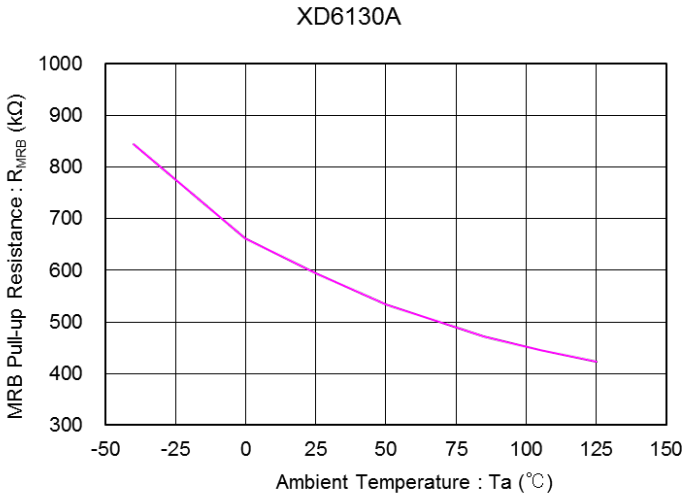


(17) ENB Low Level Threshold Voltage vs. Ambient Temperature

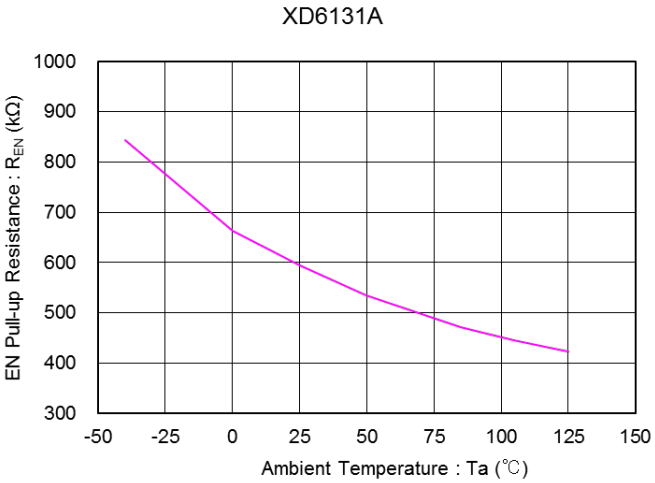


■TYPICAL PERFORMANCE CHARACTERISTICS

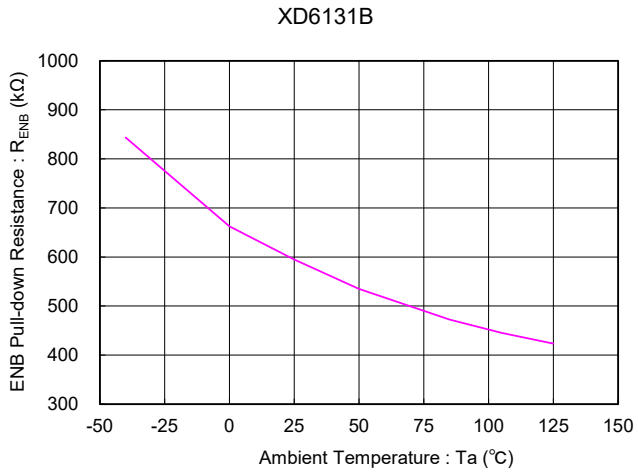
(18) MRB Pull-up Resistance vs. Ambient Temperature



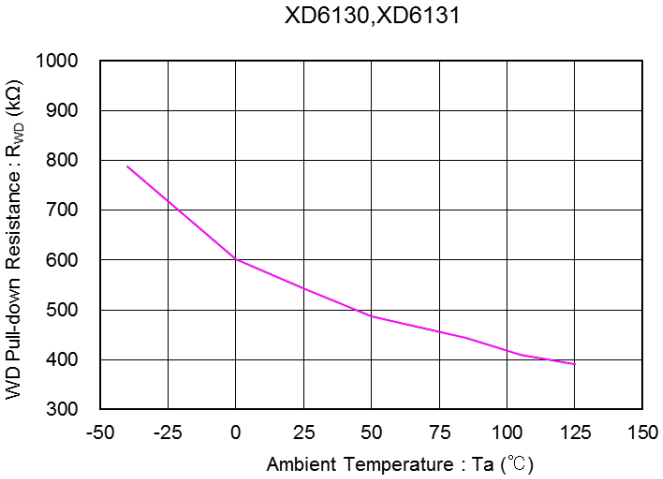
(19) EN Pull-up Resistance vs. Ambient Temperature



(20) ENB Pull-down Resistance vs. Ambient Temperature



(21) WD Pull-down Resistance vs. Ambient Temperature



■PACKAGING INFORMATION

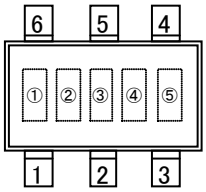
For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
SOT-26	SOT-26 PKG	SOT-26 Power Dissipation

■MARKING RULE

●XD6130 series

SOT-26



① represents products series.

MARK	PRODUCT SERIES
5	XD6130******-Q

②③ represents type of detector and detect voltage.

MARK	DETECT VOLTAGE (V)	TYPE	PRODUCT SERIES
16	1.6	A	XD6130A161MR-Q
22	2.2		XD6130A221MR-Q
23	2.3		XD6130A231MR-Q
24	2.4		XD6130A241MR-Q
29	2.9		XD6130A291MR-Q
30	3.0		XD6130A301MR-Q
31	3.1		XD6130A311MR-Q
44	4.4		XD6130A441MR-Q
45	4.5		XD6130A451MR-Q
46	4.6		XD6130A461MR-Q

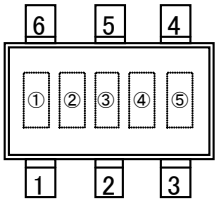
*For another marking rule of detect voltage, please contact your local Torex sales office or representative.

④⑤ represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order.
(G, I, J, O, Q, W excluded)
* No character inversion used.

■MARKING RULE

●XD6131 series

SOT-26



① represents products series.

MARK	PRODUCT SERIES
5	XD6131******-Q

②③ represents type of detector and detect voltage.

MARK	DETECT VOLTAGE (V)	TYPE	PRODUCT SERIES
A6	1.6	A	XD6131A161MR-Q
B2	2.2		XD6131A221MR-Q
B3	2.3		XD6131A231MR-Q
B4	2.4		XD6131A241MR-Q
B9	2.9		XD6131A291MR-Q
B0	3.0		XD6131A301MR-Q
C1	3.1		XD6131A311MR-Q
D4	4.4		XD6131A441MR-Q
D5	4.5		XD6131A451MR-Q
D6	4.6		XD6131A461MR-Q
E6	1.6	B	XD6131B161MR-Q
F2	2.2		XD6131B221MR-Q
F3	2.3		XD6131B231MR-Q
F4	2.4		XD6131B241MR-Q
F9	2.9		XD6131B291MR-Q
F0	3.0		XD6131B301MR-Q
H1	3.1		XD6131B311MR-Q
K4	4.4		XD6131B441MR-Q
K5	4.5		XD6131B451MR-Q
K6	4.6		XD6131B461MR-Q

*For another marking rule of detect voltage, please contact your local Torex sales office or representative.

④⑤ represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order.
(G, I, J, O, Q, W excluded)
* No character inversion used.

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