XC9519 Series

ETR0710-009a

Dual Output Step-Up/Inverting DC/DC Converter

■GENERAL DESCRIPTION

The XC9519 series is a 2 channel (step-up and inverting) DC/DC converter IC. One DC/DC converter is a step-up DC/DC and the other is an inverting DC/DC converter. The step-up converter compares a built-in reference voltage 1.0V to the FBP voltage (accuracy ±1.5%) and a positive output voltage can be set freely with the external components up to 18V. The inverting DC/DC converter compares a difference between a reference voltage and the FBN voltage (accuracy ±1.5%) to the GND, then a negative output voltage can be set until -15V with the external components.

With a 1.2MHz frequency, the size of the external components can be reduced. As for operation mode, the device can be selected to use PWM control or automatic PWM/PFM switching control by the MODE pin. In the automatic PWM/PFM switching control mode, control switches from PWM to PFM during light loads. The series is highly efficient from light loads through to large output currents. In the PWM control mode, noise is easily reduced since the frequency is fixed. The control mode can be selected for each application. The soft start and current control functions are internally optimized. During stand-by, all circuits in the IC are shutdown to reduce current consumption to as low as 1.0μA or less. The device includes a gate control pin for the P-channel MOSFET which is used for a load disconnection at the stand-by mode. The GAINP and GAINN pins are used for loop compensation in order to optimize load transient response. With the built-in UVLO (Under Voltage Lock Out) function, the internal driver transistor is forced OFF when input voltage becomes 2.2V or lower.

■APPLICATIONS

- ●AMOLED
  - Smartphones
  - Tablet PCs
  - Automotive navigation systems
- ●CCD image sensors
  - Surveillance cameras
- ●e-paper
  - -e-Books

■FEATURES

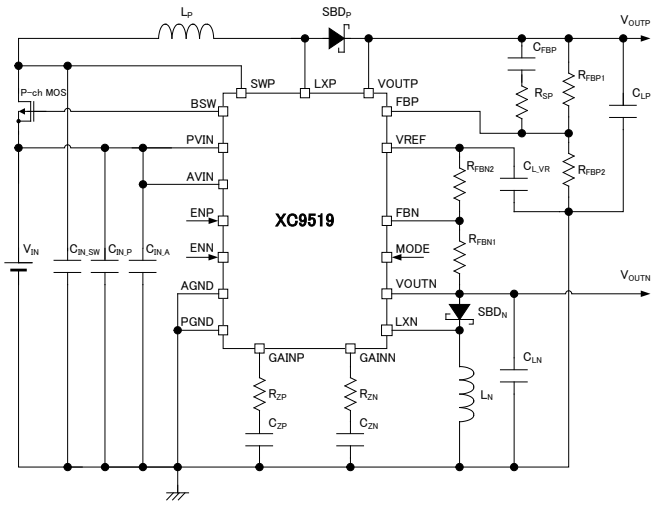
Input Voltage	: 2.7V ~ 5.5V
Output Current	: 500mA @V_{IN}=3.7V, V_{OUTP}=5.0V, V_{OUTN}=-5.0V
Positive Output Voltage	: 4.0V (*1) ~ 18.0V (accuracy ±1.5% @25°C)
Negative Output Voltage	: -15.0V (*2) ~ -4.0V (accuracy ±1.5% @25°C)
Oscillation Frequency	: 1.2MHz
Soft-Start Circuit Built-In	: Step-up DC/DC converter 2.5ms (TYP.)
	: Inverting DC/DC converter 2.2ms (TYP.)
Protection Circuits	: Over Current Limit (Integral Latching)
	Short Protection Latching
	UVLO
	Thermal Shutdown
	Over Voltage Protection
Function Addition	: Control Pin
	Load disconnect Pin
	Phase Compensation Pin
	Ceramic Capacitor Compatible
Operating Ambient Temperature	: -40°C ~ +85°C
Package	: QFN-24
Environmentally Friendly	: EU RoHS Compliant, Pb Free

(*1) $V_{OUTPSET} \geqq V_{IN}$ + 0.2V ($V_{OUTPSET}$:Positive output voltage range)

(*2) V_{IN} - $V_{OUTNSET}$+ $V_{FN} \leqq$21.0V

(V_{FN} : Forward voltage of SBD_N, $V_{OUTNSET}$: Nagative output voltage range)

■ TYPICAL APPLICATION

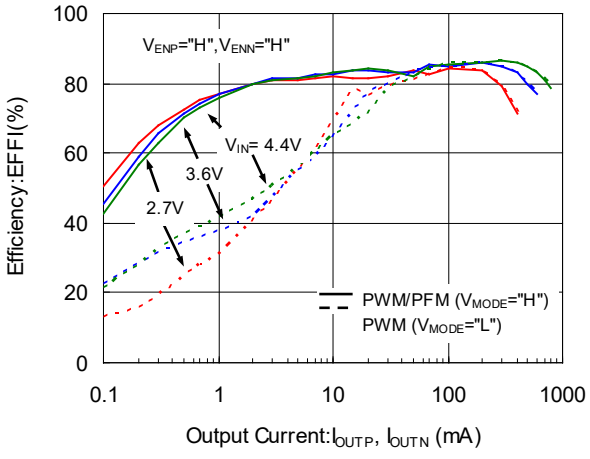


■TYPICAL PERFORMANCE CHARACTERISTICS

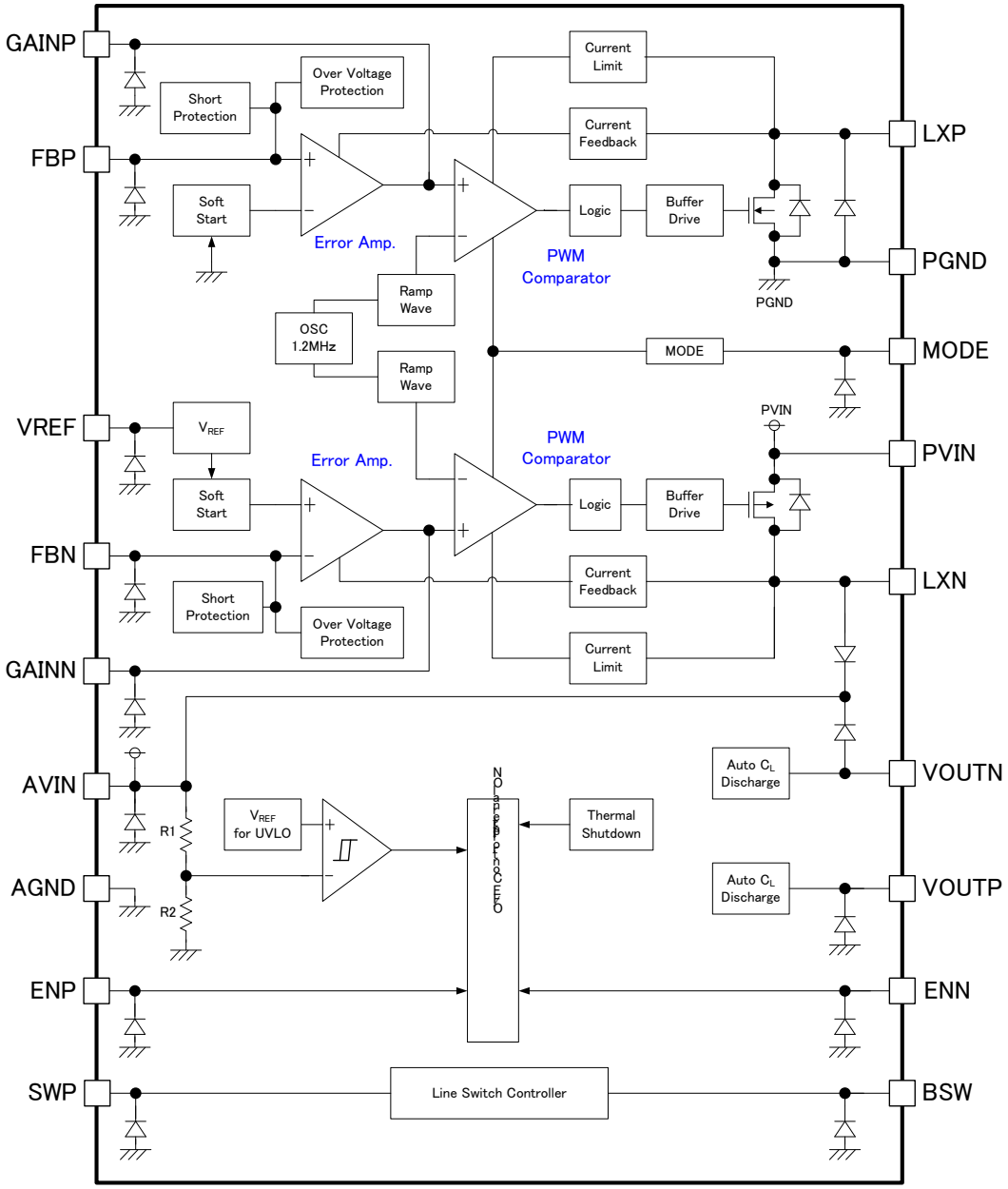
V_{OUTP}=5.0V, V_{OUTN}=-5.0V, I_{OUTP}=I_{OUTN}

C_{LP}, C_{LN}=4×4.7μF, L_P, L_N=3.3μH (VLF5014S-3R3M2R0), SBD_P, SBD_N: CMS03

P-ch MOS: EMH1303, R_{ZP}=7.5kΩ, C_{ZP}=4.7nF, R_{ZN}=130kΩ, C_{ZN}=0.47nF



■BLOCK DIAGRAM



* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

■PRODUCT CLASSIFICATION

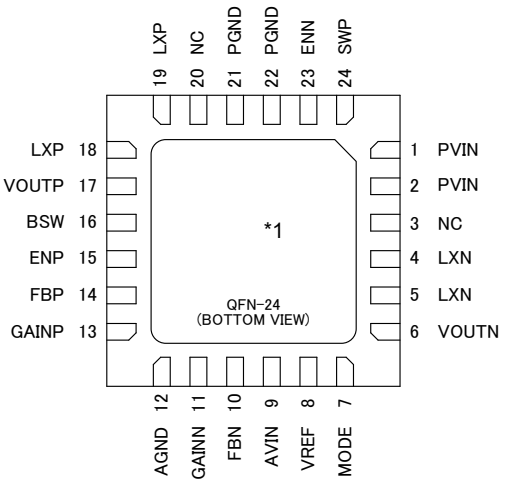
●Ordering Information

XC9519①②③④⑤⑥-⑦

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	UVLO Detect Voltage	A	UVLO Detect Voltage 2.2V UVLO Hysteresis width 0.2V
②③	Oscillation Frequency	12	1.2 MHz
④	Maximum Current Limit	A	2.0A
⑤⑥-⑦ (*1)	Package (Order Unit)	ZR-G	QFN-24 (1,000/Reel) (*2)

(*1) The “-G” suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.
(*2) The XC9519 reels are shipped in a moisture-proof packing.

■PIN CONFIGURATION



*1: The back metal pad, AGND pin and two PGND pins (No. 21 and 22) should be connected outside.

■ PIN ASSIGNMENT

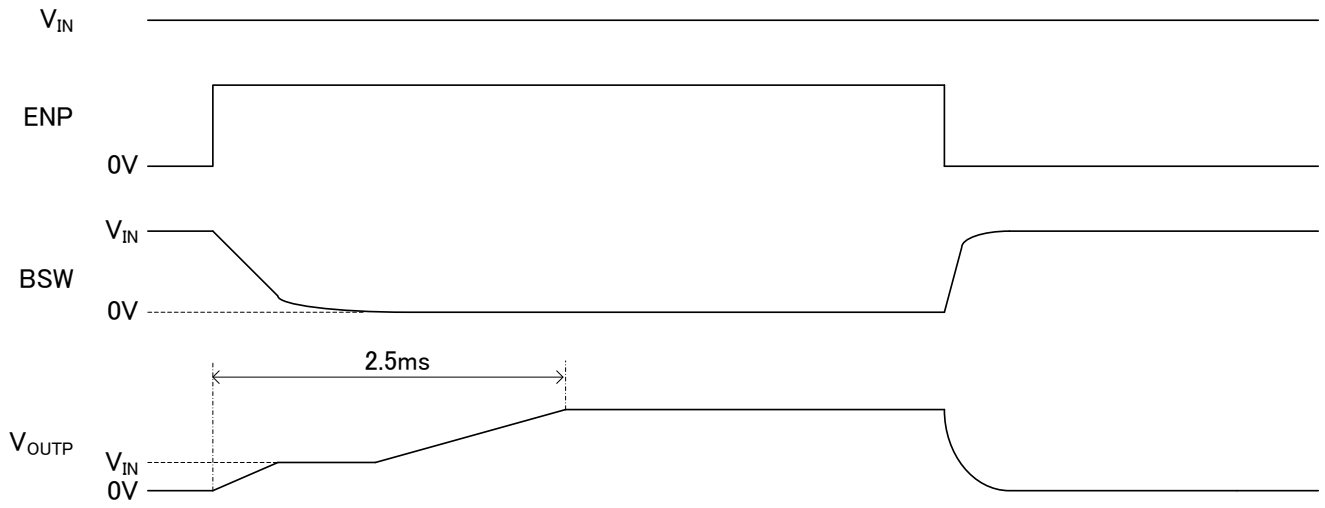
PIN NUMBER QFN-24	PIN NAME	FUNCTION
1, 2	PVIN	Power Supply Input 1
3	NC	No Connection
4, 5	LXN	Switching of Inverting DC/DC Converter
6	VOUTN	Detect Monitoring of Inverting DC/DC Output Voltage
7	MODE	Selection Pin for Control Mode
8	VREF	Reference Output Voltage
9	AVIN	Power Supply Input 2
10	FBN	Feedback Pin for Inverting DC/DC Converter
11	GAINN	Loop Compensation Pin for Inverting DC/DC Converter
12	AGND	Analog Ground
13	GAINP	Loop Compensation Pin for Step-Up DC/DC Converter
14	FBP	Feedback Pin for Step-Up DC/DC Converter
15	ENP	Chip Enable Pin for Step-Up DC/DC Converter
16	BSW	P-channel MOS FET Gate Control Pin
17	VOUTP	Output Voltage Sense for Step-Up DC/DC Converter
18, 19	LXP	Switching Output of Step-Up DC/DC Converter
20	NC	No Connection
21, 22	PGND	Power Ground
23	ENN	Chip Enable Pin for Inverting DC/DC Converter
24	SWP	Detect Monitoring Voltage Pin for P-channel MOS FET Drain

■FUNCTION

1. ENP Pin Function

ENP PIN	STATUS
H	Step-up DC/DC Converter Active
L	Step-up DC/DC Converter Stand-by

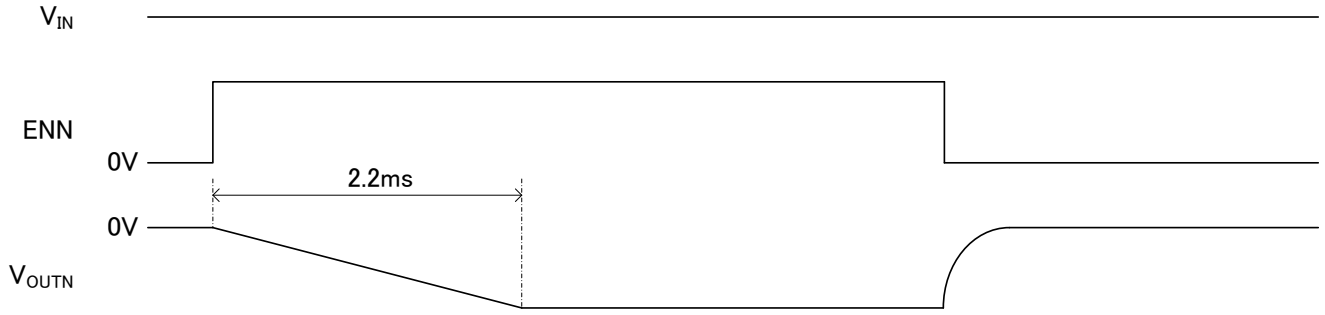
* Please do not leave the ENP pin open.



2. ENN Pin Function

ENN PIN	STATUS
H	Inverting DC/DC Converter Active
L	Inverting DC/DC Converter Stand-by

* Please do not leave the ENP pin open.



3. MODE Pin Function

MODE PIN	STATUS
H	Auto PWM/PFM
L	PWM Control

* Please do not leave the MODE pin open.

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER	SYMBOL	RATINGS	UNITS
PVIN Pin Voltage	V_{PVIN}	-0.3 ~ +6.0	V
AVIN Pin Voltage	V_{AVIN}	-0.3 ~ +6.0	V
ENP Pin Voltage	V_{ENP}	-0.3 ~ +6.0	V
ENN Pin Voltage	V_{ENN}	-0.3 ~ +6.0	V
MODE Pin Voltage	V_{MODE}	-0.3 ~ +6.0	V
LXP Pin Voltage	V_{LXP}	-0.3 ~ +22.0	V
LXN Pin Voltage	V_{LXN}	V_{PVIN} -22.0 ~ V_{PVIN} +0.3	V
FBP Pin Voltage	V_{FBP}	-0.3 ~ +6.0	V
FBN Pin Voltage	V_{FBN}	-0.3 ~ +6.0	V
VOUTP Pin Voltage	V_{OUTP}	-0.3 ~ +22.0	V
VOUTN Pin Voltage	V_{OUTN}	V_{AVIN} -22.0 ~ V_{AVIN} +0.3	V
BSW Pin Voltage	V_{BSW}	-0.3 ~ +6.0	V
SWP Pin Voltage	V_{SWP}	-0.3 ~ +6.0	V
VREF Pin Voltage	V_{REF}	-0.3 ~ +6.0	V
GAINP Pin Voltage	V_{GAINP}	-0.3 ~ +6.0	V
GAINN Pin Voltage	V_{GAINN}	-0.3 ~ +6.0	V
LXP Pin Current	I_{LXP}	4000	mA
LXN Pin Current	I_{LXN}	4000	mA
Power Dissipation	Pd	1500 (PCB mounted) *	mW
Operating Ambient Temperature	Topr	-40 ~ +85	ºC
Storage Temperature	Tstg	-55 ~ +125	ºC

* All voltages are described based on the AGND and PGND pin.
* The value is an example of data which is taken with the PCB mounted. Please refer to our web site for details.

■ELECTRICAL CHARACTERISTICS

●XC9519 Series, Common Characteristics

f_{OSC}=1.2MHz Ta=25℃

PARAMETER	SYMBOL	CONDITIONS (*1)	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Input Voltage	V_{IN}		2.7	-	5.5	V	-
UVLO Detect Voltage	V_{UVLO}	V_{ENP} =1.5V , V_{ENN} = V_{FBP} = 0V, V_{FBN} = 0.1V The voltage which L_{XP} stops oscillation while V_{IN} is decreasing from 2.4V.	2.0	2.2	2.4	V	⑨
UVLO Release Voltage	V_{UVLOR}	V_{ENP} =1.5V , V_{ENN} = V_{FBP} = 0V, V_{FBN} = 0.1V The voltage which L_{XP} starts oscillation while V_{IN} is increasing from V_{UVLO}.	2.2	2.4	2.6	V	⑨
UVLO Hysteresis Range	V_{UVLOH}	V_{UVLOH} = V_{UVLOR} - V_{UVLO}	-	0.2	-	V	-
Supply Current 1	I_{DD1}	V_{IN} =V_{ENP} = V_{ENN} = V_{MODE} = 5.5V V_{FBP} =5.5V, V_{FBN} = -0.1V, V_{OUTP} = V_{SWP} = 5.5V	50	170	450	μA	①
Supply Current 2	I_{DD2}	V_{IN} = V_{ENN} = V_{MODE} = 5.5V, V_{ENP} = 0V V_{FBN} = -0.1V	30	90	250	μA	①
Supply Current 3	I_{DD3}	V_{IN} =V_{ENP} = V_{MODE} = 5.5V, V_{ENN} =0V V_{FBP} = 5.5V, V_{OUTP} = V_{SWP} = 5.5V	30	110	250	μA	①
Stand-by Current	I_{STB}	V_{IN} =5.5V, V_{ENP} =V_{ENN} = V_{MODE} = 0V	-	0	1.0	μA	①
ENP "H" Voltage	V_{ENPH}	V_{IN} = 5.5V, V_{ENN} = V_{MODE} = 0V, V_{FBP} = 0V The voltage which L_{XP} starts oscillation while V_{ENP} is increasing from 0.3V.	1.4	-	5.5	V	⑦
ENP "L" Voltage	V_{ENPL}	V_{IN} = 5.5V, V_{ENN} = V_{MODE} = 0V, V_{FBP} = 0V The voltage which L_{XP} stops oscillation while V_{ENP} Is decreasing from 1.4V.	AGND	-	0.3	V	⑦
ENP "H" Current	I_{ENPH}	V_{IN} = V_{ENP} = 5.5V	-0.1	-	0.1	μA	⑦
ENP "L" Current	I_{ENPL}	V_{IN} = V_{ENP} = 0V	-0.1	-	0.1	μA	⑦
ENN "H" Voltage	V_{ENNH}	V_{IN} = 5.5V, V_{ENP} = V_{MODE} = 0V, V_{FBN} = 5.5V The voltage which L_{XN} starts oscillation while V_{ENN} is increasing from 0.3V.	1.4	-	5.5	V	⑦
ENN "L" Voltage	V_{ENNL}	V_{IN} = 5.5V, V_{ENP} = V_{MODE} = 0V, V_{FBN} = 5.5V The voltage which L_{XN} stops oscillation while V_{ENN} is decreasing from 1.4V.	AGND	-	0.3	V	⑦
ENN "H" Current	I_{ENNH}	V_{IN} = V_{ENN} = 5.5V	-0.1	-	0.1	μA	⑦
ENN "L" Current	I_{ENNL}	V_{IN} = V_{ENN} = 0V	-0.1	-	0.1	μA	⑦
MODE "H" Voltage	V_{MODEH}	V_{IN} = V_{ENP} = 5.5V, V_{ENN} = 0V, The voltage which supply current decreases while V_{MODE} is increasing from 0.3V.	1.4	-	5.5	V	⑦
MODE "L" Voltage	V_{MODEL}	V_{IN} = V_{ENP} = 5.5V, V_{ENN} = 0V, The voltage which supply current increases while V_{MODE} is decreasing from 1.4V.	AGND	-	0.3	V	⑦
MODE "H" Current	I_{MODEH}	V_{IN} = V_{MODE} = 5.5V	-0.1	-	0.1	μA	⑦
MODE "L" Current	I_{MODEL}	V_{IN} = V_{MODE} = 0V	-0.1	-	0.1	μA	⑦
FBP "H" Current	I_{FBPH}	V_{IN} =5.5V, V_{ENP} =V_{ENN} =V_{MODE} =0V, V_{FBP} =5.5V	-0.1	-	0.1	μA	⑦
FBP "L" Current	I_{FBPL}	V_{IN} =5.5V, V_{ENP} =V_{ENN} =V_{MODE} =0V, V_{FBP} =0V	-0.1	-	0.1	μA	⑦
FBN "H" Current	I_{FBNH}	V_{IN} =5.5V, V_{ENP} =V_{ENN} =V_{MODE} =0V, V_{FBN} =5.5V	-0.1	-	0.1	μA	⑦
FBN "L" Current	I_{FBNL}	V_{IN} =5.5V, V_{ENP} =V_{ENN} =V_{MODE} =0V, V_{FBN} =0V	-0.1	-	0.1	μA	⑦
SWP "H" Current	I_{SWPH}	V_{IN} =5.5V, V_{ENP} =V_{ENN} =V_{MODE} =0V, V_{SWP} =5.5V	-0.1	-	0.1	μA	⑦
SWP "L" Current	I_{SWPL}	V_{IN} =5.5V, V_{ENP} =V_{ENN} =V_{MODE} =0V, V_{SWP} =0V	-0.1	-	0.1	μA	⑦
Integral Latch Time	t_{LAT}	V_{IN} =V_{ENP} =V_{ENN} = 5.5V, V_{MODE} =0V V_{FBP} =0.9V, V_{FBN} = 0.1V Time to stop operation from the start of maximum current limit status.	1.0	2.0	3.0	ms	⑤
Thermal Shutdown Temperature	T_{TSD}		-	150	-	℃	-
Thermal Shutdown Release Temperature	T_{TSDR}		-	130	-	℃	-
Thermal Shutdown Hysteresis Range	T_{HYS}	T_{HYS} =T_{TSDR} - T_{TSD}	-	20	-	℃	-

(*1) If the applied voltage and its pin name are not stated, those pins are left open for measurement.

■ELECTRICAL CHARACTERISTICS (Continued)

●XC9519 Series, Step-up DC/DC Converter

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS (*1)	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage Range	$V_{OUTPSET}$		4.0 (*2)	-	18.0	V	-
FBP Voltage	V_{FBP}	V_{IN} = V_{ENP} = 3.6V, V_{ENN} = V_{MODE} = 0V V_{OUTP} = V_{SWP} = 3.6V The voltage which L_{XP} starts oscillation while V_{FBP} is decreasing.	0.985	1.000	1.015	V	③
Oscillation Frequency	f_{OSCP}	V_{IN} = V_{ENP} = 3.6V, V_{ENN} = V_{MODE} = 0V V_{OUTP} = V_{SWP} = 3.6V, V_{FBP} =0V	1020	1200	1380	kHz	③
PFM Switching Current	I_{PFMP}	V_{IN} =V_{ENP} = V_{MODE} = 3.6V, V_{ENN} =0V	180	350	550	mA	⑧
Maximum Duty Cycle	D_{MAXP}	V_{IN} = V_{ENP} = 3.6V, V_{ENN} = V_{MODE} = 0V V_{OUTP} = V_{SWP} = 3.6V, V_{FBP} =0V	84	90	97	%	③
LXP SW “H” ON Resistance	R_{LXPH}	V_{IN} = V_{ENP} = 3.6V, V_{ENN} = V_{MODE} = 0V, I_{LXP} = 100mA	-	0.12	0.28	Ω	④
LXP SW “H” Leak Current	I_{LEAKH}	V_{IN} =5.5V, V_{ENP}=0V, V_{LXP}=5.5V	-	0.01	1.0	μA	⑥
Maximum Current Limit (*3)	I_{LIMP}	V_{IN} =V_{ENP} = 5.5V, V_{ENN} = V_{MODE} =0V V_{FBP} = 0.9V, V_{OUTP} = V_{SWP} = 5.5V	2000	-	4000	mA	⑤
FBP Voltage Temperature Characteristics	$\triangle V_{FBP}$ / (V_{FBP} ・ $\triangle$Topr)	-40 ℃≦Topr≦85 ℃	-	±100	-	ppm / ℃	-
Soft-Start Time	t_{SSP}	V_{IN} = 3.6V, V_{ENN} = V_{MODE} = 0V V_{OUTP} = V_{SWP} = 3.6V, V_{FBP} = 0.95V Time to start L_{XP} oscillation from the rise of V_{ENP}. (0V→3.6V)	0.8	2.5	5.2	ms	③
Short Protection Threshold Voltage	V_{SHORTP}	V_{IN} =V_{ENP} = 5.5V, V_{ENN} = V_{MODE} =0V V_{OUTP} = V_{SWP} = 5.5V The voltage which the integral latch time becomes 200μs or less while V_{FBP} is decreasing.	0.3	0.5	0.7	V	⑤
Over Voltage Protection Limit	V_{OVPP}	V_{IN} = V_{ENP} = 3.6V, V_{ENN} = V_{MODE} = 0V V_{OUTP} = V_{SWP} = 3.6V, V_{GAINP} = 3.6V The voltage which L_{XP} stops oscillation while V_{FBP} is increasing.	V_{FBP} +0.03	V_{FBP} +0.07	V_{FBP} +0.10	V	③
BSW Pin Current	I_{BSW}	V_{IN} = V_{ENP} = 3.6V, V_{ENN} = V_{MODE} = 0V V_{OUTP} = V_{SWP} = 3.6V, V_{BSW} =3.6V	0.2	1.2	3.0	mA	⑦
C_L Discharge Resistance	R_{DCHGP}	V_{IN} = 6.0V, V_{ENP} =V_{ENN} = V_{MODE} = 0V V_{OUTP} = 4.0V	50	200	500	Ω	②

NOTE:

(*1) If the applied voltage and its pin name are not stated, those pins are left open for measurement.

(*2) Input voltage or positive output voltage range should be $V_{OUTPSET}$≧V_{IN} + 0.2V.

(*3) Maximum current limit denotes the level of detection at peak of coil current.

■ELECTRICAL CHARACTERISTICS (Continued)

●XC9519 Series, Inverting DC/DC Converter

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS (*1)	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage Range	$V_{OUTNSET}$		-15.0(*2)	-	-4.0	V	-
FBN Voltage	V_{FBN}	V_{IN} = V_{ENN} = 3.6V, V_{ENP} = V_{MODE} = 0V The voltage which L_{XN} starts oscillation while V_{FBN} is increasing.	-26	0	26	mV	③
Reference Voltage	V_{REF}	V_{IN} = V_{ENN} = 3.6V, V_{ENP} = V_{MODE} = 0V, V_{FBN}= 0.1V	0.970	1.000	1.030	V	①
Output Voltage Accuracy	V_{OUTNA}	V_{OUTNA} =V_{REF} -V_{FBN}	0.985	1.000	1.015	V	-
Oscillation Frequency	f_{OSCN}	V_{IN} = V_{ENN} = 3.6V, V_{ENP} = V_{MODE} = 0V, V_{FBN}= 0.1V	1020	1200	1380	kHz	③
PFM Switching Current	I_{PFMN}	V_{IN} = V_{ENN} = V_{MODE} = 3.6V, V_{ENP} = 0V	220	350	550	mA	⑧
Maximum Duty Cycle	D_{MAXN}	V_{IN} = V_{ENN} = 3.6V, V_{ENP} = V_{MODE} = 0V, V_{FBN}= 0.1V	84	90	97	%	③
LXN SW “L” ON Resistance	R_{LXNL}	V_{IN} = V_{ENN} = 3.6V, V_{ENP} = V_{MODE} = 0V, I_{LXN} = 100mA	-	0.22	0.48	Ω	④
LXN SW “L” Leak Current	I_{LEAKL}	V_{IN} = V_{ENN} = 3.6V, V_{ENP} = V_{MODE} = 0V, V_{FBN}= 0.1V	-	0.01	1.0	μA	⑥
Maximum Current Limit (*3)	I_{LIMN}	V_{IN} = V_{ENN} = 5.5V, V_{ENP} = V_{MODE} = 0V V_{FBN} = 0.1V	2000	-	4000	mA	⑤
Reference Voltage Temperature Characteristics	$\triangle V_{REF}$ / (V_{REF} ・ $\triangle$Topr)	-40 °C≦Topr≦85 °C	-	±100	-	ppm / °C	-
Soft-Start Time	t_{SSN}	V_{IN} = 3.6V, V_{ENP} = V_{MODE} = 0V, V_{FBN} = 0.05V Time to start L_{XN} oscillation from the rise of V_{ENP}. (0V→3.6V)	0.8	2.2	4.0	ms	③
Short Protection Threshold Voltage	V_{SHORTN}	V_{IN} = V_{ENN} = 5.5V, V_{ENP} = V_{MODE} = 0V The voltage which the integral latch time becomes 200μs or less while V_{FBN} is increasing.	0.3	0.5	0.7	V	⑤
Over Voltage Protection Limit	V_{OVPN}	V_{IN} = V_{ENN} = 3.6V, V_{ENP} = V_{MODE} = 0V, V_{GAINN} = 3.6V The voltage which L_{XN} stops oscillation while V_{FBN} is decreasing.	V_{FBN} -0.10	V_{FBN} -0.07	V_{FBN} -0.03	V	③
C_L Discharge Resistance	R_{DCHGN}	V_{IN} = 6.0V, V_{ENP} =V_{ENN} = V_{MODE} = 0V V_{OUTN} = -4.0V	50	200	500	Ω	②

NOTE:

(*1) If the applied voltage and its pin name are not stated, those pins are left open for measurement.

(*2) Input voltage or positive output voltage range should be V_{IN} - $V_{OUTNSET}$+ V_{FN}≦21.0V (V_{FN}: Forward voltage of external schottky barrier diode) .

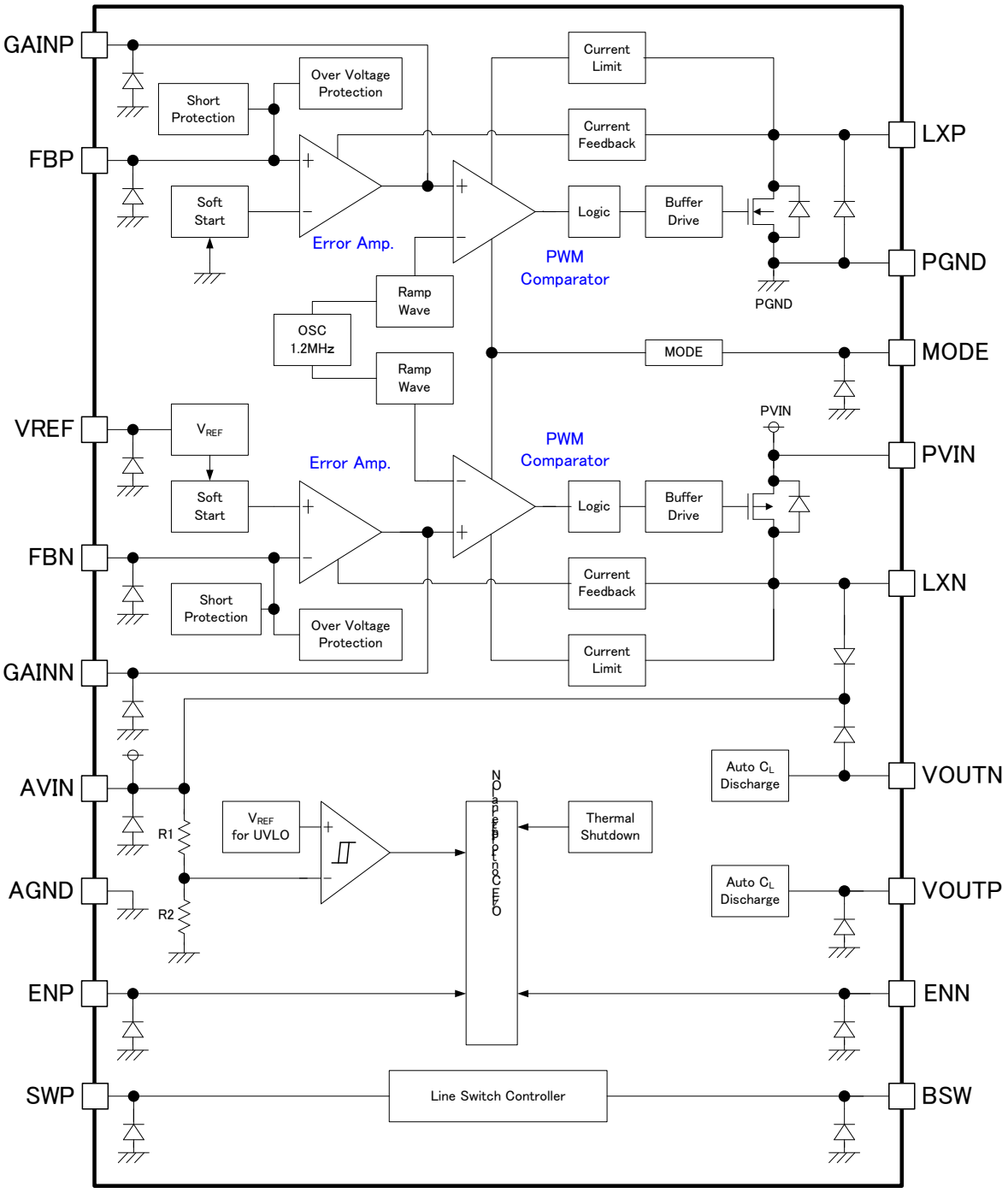
(*3) Maximum current limit denotes the level of detection at peak of coil current.

■OPERATIONAL EXPLANATION

The XC9519 series consists of a reference voltage source, ramp wave circuit, error amplifier, PWM comparator, phase compensation circuit, driver transistor, current limiter circuit, short protection circuit, UVLO circuit, thermal shutdown circuit, over voltage protection, load disconnect control and others. (See the block diagram below.)

By using the error amplifier, the FBP (FBN) pin voltage is compared with the internal reference voltage. The error amplifier output is sent to the PWM comparator in order to determine the duty cycle of PWM switching. The signal from the error amplifier is compared with the ramp wave from the ramp wave circuit, and the resulting output is delivered to the buffer driver circuit to provide on-time of the duty cycle at the LXP (LXN) pin. This process is continuously performed to ensure stable output voltage.

The current feedback circuit monitors the driver transistor current for each switching operation, and modulates the error amplifier output signal to provide multiple feedback signals. This enables a stable feedback loop even when using a low ESR capacitor such as ceramic, which results in ensuring stable output voltage.



* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

■OPERATIONAL EXPLANATION (Continued)

<Reference Voltage Source>

The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

<Step-up DC/DC Converter Error Amplifier>

The step-up DC/DC converter error amplifier is an amplifier for output voltage monitoring. The FBP pin voltage is compared to the reference voltage. When a voltage lower than the reference voltage is feedback to the FBP pin voltage, the output voltage of the error amplifier goes high. External compensation of the error amplifier frequency characteristic is also possible.

<Inverting DC/DC Converter Error Amplifier>

The inverting DC/DC converter error amplifier is an amplifier for output voltage monitoring. The FBN pin voltage is compared to GND. When a voltage higher than GND is feedback to the FBN pin voltage, the output voltage of the error amplifier goes high. External compensation of the error amplifier frequency characteristic is also possible.

<Ramp Wave Circuit>

The ramp wave circuit determines switching frequency. The frequency is fixed 1.2MHz internally. Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation, and to synchronize all the internal circuits.

<UVLO Circuit>

When the AVIN pin voltage becomes 2.2V or lower, the driver transistor is forced OFF to prevent false pulse output caused by unstable operation of the internal circuitry. When the AVIN pin voltage becomes 2.4V or higher, switching operation takes place. By releasing the UVLO function, the IC performs the soft start function to initiate output startup operation. The soft start function operates even when the AVIN pin voltage falls momentarily below the UVLO detect voltage. The UVLO circuit does not cause a complete shutdown of the IC, but causes pulse output to be suspended; therefore, the internal circuitry remains in operation.

<Thermal Shutdown>

For protection against heat damage of the ICs, thermal shutdown function monitors chip temperature. The thermal shutdown circuit starts operating and the driver transistor will be turned off when the chip's temperature reaches 150 °C. When the temperature drops to 130 °C or less after shutting of the current flow, the IC performs the soft start function to initiate output startup operation.

<PFM Switch Current>

In PFM control operation, until coil current reaches to a specified level (I_{PFMP}, I_{PFMN}), the IC keeps the driver transistor on. In this case, time (t_{ON}) that the driver transistor is kept on can be given by the following formula.

$t_{ON} = L \times I_{PFMP}\ (I_{PFMN}) / V_{IN}$

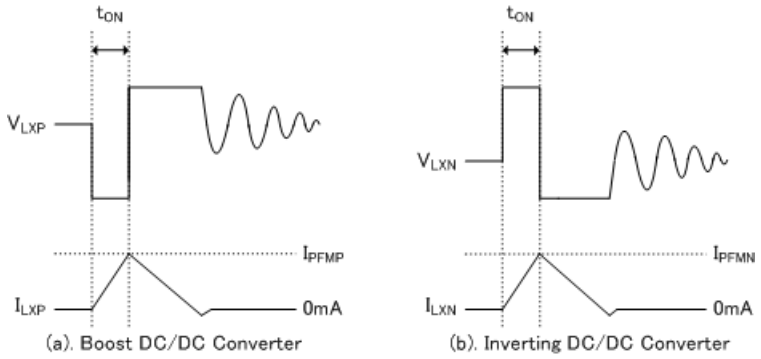


Fig. PFM Current

< PFM Duty Limit >

In PFM control operation, the maximum duty cycle (DTY_{LIMIT_PFM}) is set to 50% (TYP.). Therefore, under the condition that the duty increases (e.g. the condition that the step-up ratio is large), it's possible for the driver transistor to be turned off even when the coil current doesn't reach to I_{PFMP} (I_{PFMN}).

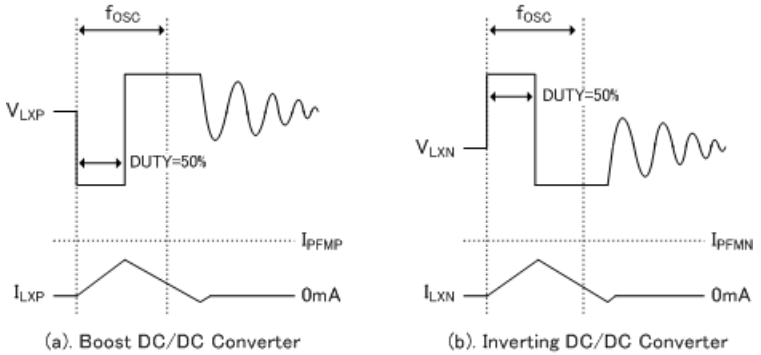


Fig. Maximum PFM Current Duty

■OPERATIONAL EXPLANATION (Continued)

< C_L Auto-Discharge Function >

This function enables high-speed discharge of the charge on the output capacitor (C_L) when an L level signal is input to the ENP (ENN) pin by means of the internal switch between the VOUTP pin and AGND pin (between the VOUTN pin and AVIN pin).

This function makes it possible to prevent malfunctioning of applications caused by charge remaining on C_L.

The discharge time is determined by the C_L discharge resistance (R_{DCHC}) and C_L. If τ ($\tau = C_L \times R_{DCHG}$) is the time constant of C_L and R_{DCHG}, the equation for the output voltage discharge time can be obtained from the following CR discharge equation.

$$t = \tau \ln (V_{OUTSET} / V)$$

V: Output voltage during discharge

V_{OUTSET}: Output voltage

t: Discharge time

τ : $C_L \times R_{DCHG}$

[Example]

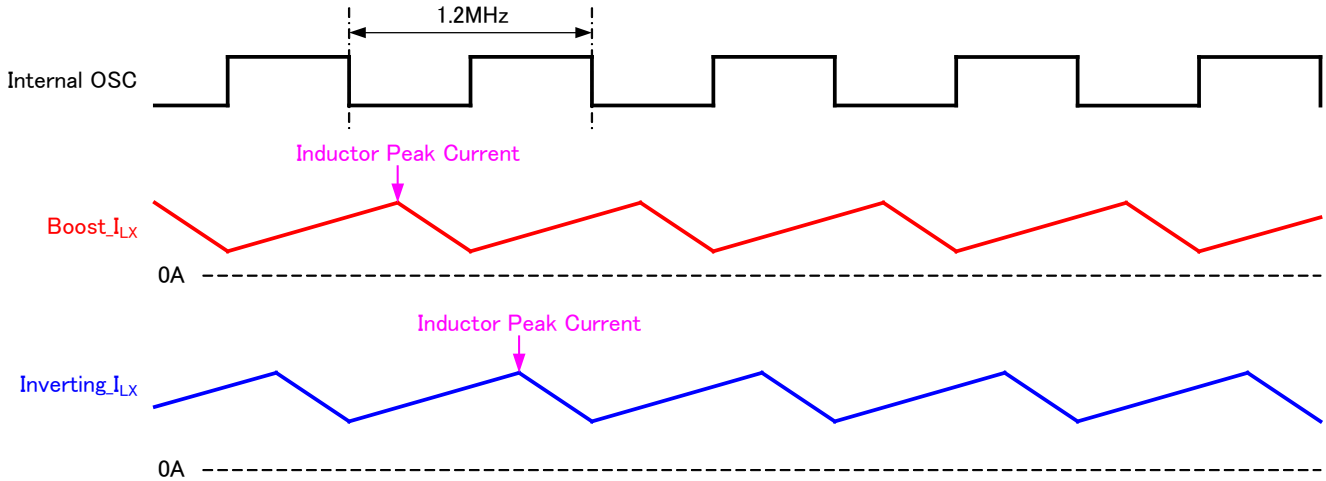
When the set voltage ($V_{OUTPSET}$)=5.0V, C_{LP}=18.8μF, and the C_L discharge resistance (R_{DCHGP})=200Ω (TYP.) of the DC/DC Converter, the discharge time t from the start of C_L high-speed discharge until the output voltage falls to 1.0V can be calculated as follows:

$$t = \tau \ln (V_{OUTPSET} / V) = C_{LP} \times R_{DCHGP} \ln (V_{OUTPSET} / V) = 18.8\mu F \times 200\Omega \times \ln (5.0V / 1.0V) = 6.05 \times 10^{-3} s = 6.05 ms$$ (*1)

(*1) Calculated with I_{OUT} = 0mA

<Internal OSC Timing Chart>

The step-up DC/DC Converter and the Inverting DC/DC Converter are switching synchronously based on one internal clock. The phase of the step-up driver on timing for the DC/DC Converter is shifted to completely opposite position (180 degrees different) upon the phase of driver on timing for the Inverting DC/DC Converter.



<Overvoltage Protection>

Overvoltage protection monitors the output voltage V_{OUTP} (V_{OUTN}) using the FBP (FBN) pin voltage, and prevents the output voltage V_{OUTP} (V_{OUTN}) from rising too far above the set voltage. In particular, fluctuations in the load cause the output voltage to rise, and when the FBP (FBN) pin voltage reaches the overvoltage protection detection voltage, the driver transistor of the step-up DC/DC converter (inverting DC/DC converter) is turned off to hold down the rise of output voltage. When the output voltage falls after overvoltage protection detection, normal DC/DC converter operation resumes.

The output voltage V_{OUT_OVP} that is detected by overvoltage protection is obtained from the following equation:

$$V_{OUT_OVPP} (V_{OUT_OVPN}) = V_{OUTPSET} (V_{OUTNSET}) \times V_{OVPP} (V_{OVPN})$$

$V_{OUTPSET}$ ($V_{OUTNSET}$): Output voltage, V_{OVPP}(V_{OVPN}): Detect Overvoltage Protection Voltage

[Example]

In a step-up DC/DC converter with the indicated conditions, the output voltage V_{OUT_OVPP} that is detected by overvoltage protection can be calculated as shown below.

Condition: Output Voltage ($V_{OUTPSET}$)=5.0V, V_{OVPP}=V_{FBP}+0.07V(TYP.) , V_{FBP}=1.0V(TYP.)

$$V_{OUT_OVPP} = V_{OUTPSET} \times V_{OVP} = 5.0V \times (1.0 + 0.07(TYP.)) = 5.0V \times 1.07 = 5.35V$$

<Load disconnect Control Circuit>

The Load disconnect control circuit makes it possible to break continuity between V_{IN} and V_{OUTP} by turning off the external P-ch MOS FET when the step-up DC/DC converter is in the standby state.

■OPERATIONAL EXPLANATION (Continued)

<Current Limit>

The current limiter circuit of the XC9519 series monitors the current flowing through the driver transistor, and features a combination of the current limit mode and the operation suspension mode.

① When the driver current is greater than a specific level, the current limit function operates to turn off the pulses from the LXP (LXN) pin at any given timing.

② When the driver transistor is turned off, the limiter circuit is then released from the current limit detection state.

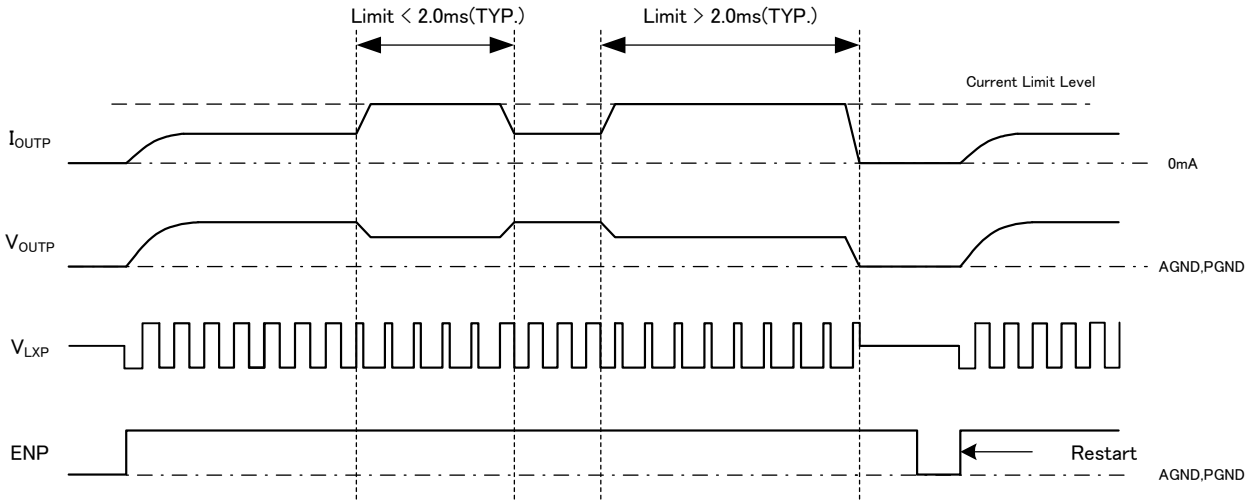
③ At the next pulse, the driver transistor is turned on. However, the transistor is immediately turned off in the case of an over current state.

④ When the over current state is eliminated, the IC resumes its normal operation.

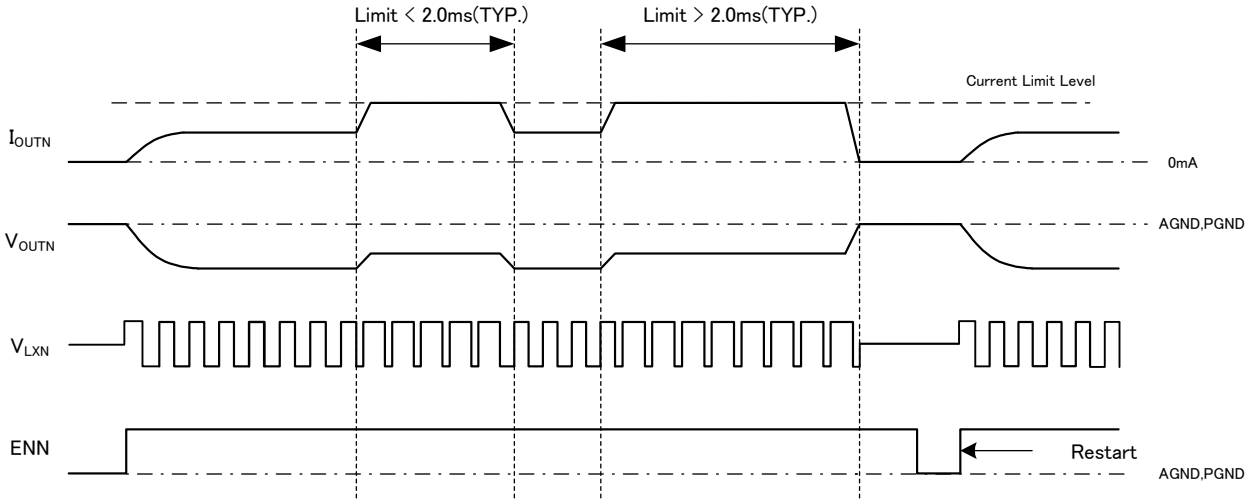
The IC waits for the over current state to end by repeating the steps ① through ③. If an over current state continues for the integral latch time and the above three steps are repeatedly performed, the IC performs the function of integral latching the OFF state of the driver transistor, and goes into operation suspension mode.

Once the IC is in suspension mode, operations can be resumed by either turning the IC off via the ENP (ENN) pin, or by restoring power. Care must be taken when laying out the PC Board, in order to prevent misoperation of the current limit mode. Depending on the state of the PC Board, latch time may become longer and latch operation may not work. In order to avoid the effect of noise, the board should be laid out so that input capacitors are placed as close to the IC as possible.

(a) Step-up DC/DC Converter



(b) Inverting DC/DC Converter



<Short-Circuit Protection>

The short-circuit protection circuit monitors the output voltage from the V_{OUTP} (V_{OUTN}). In case where output is accidentally shorted to the GND and when the FBP voltage decreases less than short protection threshold voltage or FBN pin voltage becomes larger than short protection threshold voltage and a current more than the I_{LIM} flows to the driver transistor, the short-circuit protection quickly operates to turn off and to latch the driver transistor.

Once the IC is in suspension mode, operations can be resumed by either turning the IC off via the ENP (ENN) pin, or by restoring power.

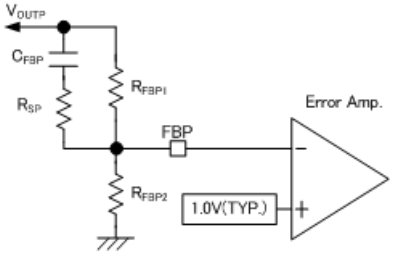
■EXTERNAL COMPONENTS

<Step-up DC/DC Converter Output Voltage Setting>

The output voltage V_{OUTP} of a step-up DC/DC converter can be set by connecting external dividing resistors R_{FBP1} and R_{FBP2}.
The output voltage V_{OUTP} is determined by the values of R_{FBP1} and R_{FBP2} as given in the equation below.
Adjust R_{FBP1} and R_{FBP2} so that $(R_{FBP1} + R_{FBP2}) < 500k\Omega$.

$$V_{OUTP} = V_{FBP} \times (R_{FBP1} + R_{FBP2}) / R_{FBP2}$$

Set the output voltage so that $V_{OUTP} \geqq V_{IN} + 0.2V$ is satisfied.



Adjust the value of the phase compensation speed-up capacitor C_{FBP} so that $f_{zfp}=1 / (2 \times \pi \times R_{FBP1})$ is about 40kHz, and insert several kΩ in series as R_{SP}. If a high output voltage is set, inserting a phase compensation speed-up capacitor may cause unstable operation.
Examples of setting C_{FBP} and R_{SP} are shown in the next section, “Step-up DC/DC Converter Error Amplifier External Compensation”.

【Typical Examples】

V_{OUTP}	R_{FBP1}	R_{FBP2}
4.0V	300kΩ	100kΩ
5.0V	300kΩ	75kΩ
9.0V	240kΩ	30kΩ
12.0V	330kΩ	30kΩ
15.0V	336kΩ	24kΩ
18.0V	408kΩ	24kΩ

<Inverting DC/DC Converter Output Voltage Setting>

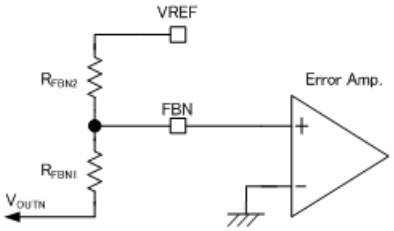
The output voltage V_{OUTN} of an inverting DC/DC converter can be set by connecting external dividing resistors R_{FBN1} and R_{FBN2}.
The output voltage V_{OUTN} is determined by the values of R_{FBN1} and R_{FBN2} as given in the equation below.
Adjust R_{FBN1} and R_{FBN2} so that $(R_{FBN1} + R_{FBN2}) < 500k\Omega$.

$$V_{OUTN} = - (V_{REF} - V_{FBN}) \times R_{FBN1} / R_{FBN2}$$

Set the output voltage so that

$$V_{IN} - V_{OUTN} + V_{FN} \leqq 21.0V$$

(V_{FN} : Forward voltage of external diode SBD_N) is satisfied.



【Typical Examples】

V_{OUTN}	R_{FBN1}	R_{FBN2}
-4.0V	300kΩ	75kΩ
-5.0V	300kΩ	60kΩ
-9.0V	270kΩ	30kΩ
-12.0V	360kΩ	30kΩ
-15.0V	360kΩ	24kΩ

■COMPONENT SELECTION METHOD (Continued)

<Step-up DC/DC Converter Error Amplifier External Compensation>

External compensation of the frequency characteristic of a step-up DC/DC converter error amplifier is possible with R_{ZP} and C_{ZP}. The values of R_{ZP} and C_{ZP} can be adjusted to obtain the optimum load-transient response (step response). For adjustment using the input voltage and output voltage, use the setting values below.

V_{IN}	Output Voltage Range	L_P	C_{LP}	R_{ZP}	C_{ZP}	C_{FBP}	R_{SP}
Li-ion (2.7～4.4V)	4.6V ≦ V_{OUTP} ≦ 5.0V	3.3μH	2×4.7μF	5.1kΩ	4.7nF	47pF(*1)	4.7kΩ
			4×4.7μF	8.2kΩ	4.7nF	47pF(*1)	4.7kΩ
	5.0V < V_{OUTP} ≦ 9.0V	3.3μH	2×4.7μF	5.1kΩ	4.7nF	-	-
			4×4.7μF	7.5kΩ	4.7nF	-	-
	9.0V < V_{OUTP} ≦ 12.0V	3.3μH	2×4.7μF	10kΩ	4.7nF	-	-
			4×4.7μF	18kΩ	2.2nF	-	-
	12.0V < V_{OUTP} ≦ 15.0V	3.3μH	2×4.7μF	16kΩ	2.2nF	-	-
			4×4.7μF	27kΩ	2.2nF	-	-
	15.0V < V_{OUTP} ≦ 18.0V	3.3μH	2×4.7μF	16kΩ	2.2nF	-	-
			4×4.7μF	24kΩ	4.7nF	-	-

V_{IN}	Output Voltage Range	L_P	C_{LP}	R_{ZP}	C_{ZP}	C_{FBP}	R_{SP}
3.3V±10%	4.0V ≦V_{OUTP} ≦ 5.0V	3.3μH	2×4.7μF	8.2kΩ	4.7nF	47pF(*2)	4.7kΩ
			4×4.7μF	13kΩ	4.7nF	47pF(*2)	4.7kΩ
	5.0V < V_{OUTP} ≦ 9.0V	3.3μH	2×4.7μF	16kΩ	2.2nF	-	-
			4×4.7μF	22kΩ	2.2nF	-	-
	9.0V < V_{OUTP} ≦12.0V	3.3μH	2×4.7μF	18kΩ	2.2nF	-	-
			4×4.7μF	30kΩ	2.2nF	-	-
	12.0V < V_{OUTP} ≦ 15.0V	3.3μH	2×4.7μF	24kΩ	2.2nF	-	-
			4×4.7μF	36kΩ	2.2nF	-	-
	15.0V < V_{OUTP} ≦ 18.0V	3.3μH	2×4.7μF	22kΩ	2.2nF	-	-
			4×4.7μF	36kΩ	2.2nF	-	-

V_{IN}	V_{OUTP}	L_P	C_{LP}	R_{ZP}	C_{ZP}	C_{FBP}	R_{SP}
5V±10%	5.7V ≦ V_{OUTP} ≦ 7.0V	3.3μH	2×4.7μF	4.7kΩ	4.7nF	68pF(*3)	4.7kΩ
			4×4.7μF	8.2kΩ	4.7nF	68pF(*3)	4.7kΩ
	7.0V < V_{OUTP} ≦ 9.0V	3.3μH	2×4.7μF	5.1kΩ	4.7nF	-	-
			4×4.7μF	10kΩ	4.7nF	-	-
	9.0V < V_{OUTP} ≦ 12.0V	3.3μH	2×4.7μF	8.2kΩ	4.7nF	-	-
			4×4.7μF	16kΩ	2.2nF	-	-
	12.0V < V_{OUTP} ≦ 15.0V	3.3μH	2×4.7μF	13kΩ	2.2nF	-	-
			4×4.7μF	24kΩ	2.2nF	-	-
	15.0V < V_{OUTP} ≦ 18.0V	3.3μH	2×4.7μF	12kΩ	2.2nF	-	-
			4×4.7μF	18kΩ	4.7nF	-	-

(*1) Setting value with RFBP1 = 300kΩ
(*2) Setting value with RFBP1 = 360kΩ
(*3) Setting value with RFBP1 = 240kΩ

■COMPONENT SELECTION METHOD (Continued)

<Inverting DC/DC Converter Error Amplifier External Compensation>

External compensation of the frequency characteristic of an inverting DC/DC converter error amplifier is possible with R_{ZN} and C_{ZN}. The values of R_{ZN} and C_{ZN} can be adjusted to obtain the optimum load-transient response (step response). For adjustment using the input voltage and output voltage, use the setting values below.

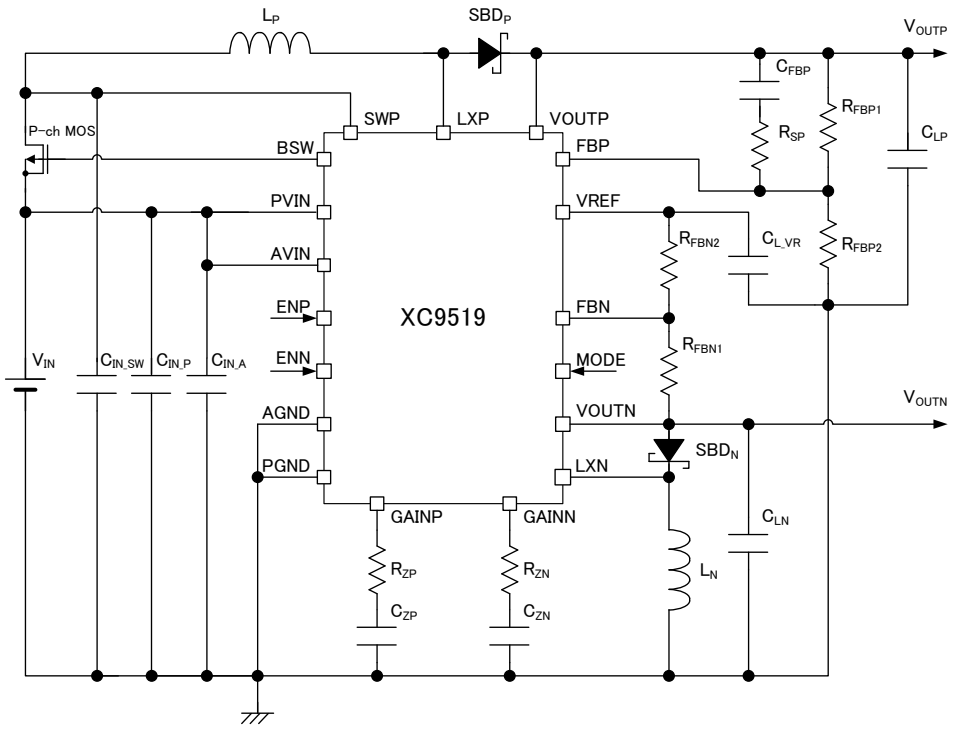
V_{IN}	Output Voltage Range	L_N	C_{LN}	R_{ZN}	C_{ZN}
Li-ion (2.7～4.4V)	-4.0V≧V_{OUTN}≧-5.0V	3.3μH	2×4.7μF	51kΩ	1.0nF
			4×4.7μF	110kΩ	0.47nF
	-5.0V > V_{OUTN}≧-9.0V	3.3μH	2×4.7μF	68kΩ	0.47nF
			4×4.7μF	130kΩ	0.47nF
	-9.0V > V_{OUTN}≧-12.0V	3.3μH	2×4.7μF	120kΩ	0.47nF
			4×4.7μF	200kΩ	0.47nF
	-12.0V > V_{OUTN}≧ -15.0V	3.3μH	2×4.7μF	110kΩ	1.0nF
			4×4.7μF	200kΩ	0.47nF

V_{IN}	Output Voltage Range	L_N	C_{LN}	R_{ZN}	C_{ZN}
3.3V±10%	-4.0V≧V_{OUTN}≧-5.0V	3.3μH	2×4.7μF	51kΩ	1.0nF
			4×4.7μF	110kΩ	0.47nF
	-5.0V > V_{OUTN}≧-9.0V	3.3μH	2×4.7μF	68kΩ	0.47nF
			4×4.7μF	130kΩ	0.47nF
	-9.0V > V_{OUTN}≧-12.0V	3.3μH	2×4.7μF	120kΩ	0.47nF
			4×4.7μF	200kΩ	0.47nF
	-12.0V > V_{OUTN}≧-15.0V	3.3μH	2×4.7μF	110kΩ	1.0nF
			4×4.7μF	200kΩ	0.47nF

V_{IN}	Output Voltage Range	L_N	C_{LN}	R_{ZN}	C_{ZN}
5V±10%	-4.0V≧V_{OUTN}≧-5.0V	3.3μH	2×4.7μF	51kΩ	1.0nF
			4×4.7μF	110kΩ	0.47nF
	-5.0V > V_{OUTN}≧-9.0V	3.3μH	2×4.7μF	68kΩ	0.47nF
			4×4.7μF	130kΩ	0.47nF
	-9.0V > V_{OUTN}≧-12.0V	3.3μH	2×4.7μF	120kΩ	0.47nF
			4×4.7μF	200kΩ	0.47nF
	-12.0V > V_{OUTN}≧-15.0V	3.3μH	2×4.7μF	110kΩ	1.0nF
			4×4.7μF	200kΩ	0.47nF

■TYPICAL APPLICATION CIRCUIT

(V_{IN}=3.6V, V_{OUTP}=5.0V, V_{OUTN}=-5.0V)



<Typical Examples> V_{IN}=3.6V, V_{OUTP}=5.0V, V_{OUTN}=-5.0V

・ Capacitor

C_{IN_P}	: 10μF/ 10V (C2012JB1A106M, TDK-EPC)
C_{IN_SW}	: 4.7μF/ 10V (C2012JB1A475M, TDK-EPC)
C_{IN_A}	: 0.1μF/ 10V (C1005JB1A104K, TDK-EPC)
C_{LP}	: 4×4.7μF/ 10V (C2012JB1A475M, TDK-EPC)
C_{LN}	: 4×4.7μF/ 10V (C2012JB1A475M, TDK-EPC)
C_{L_VR}	: 0.22μF/ 6.3V (C1005JB0J224M, TDK-EPC)
C_{ZP}	: 4.7nF/ 25V (C1005JB1E472K, TDK-EPC)
C_{ZN}	: 0.47nF/ 50V (C1005JB1H471K, TDK-EPC)
C_{FBP}	: 47pF/ 50V (C1005CH1H470J, TDK-EPC)

For C_{IN_P}, C_{IN_SW}, C_{IN_A}, C_{L_VR}, C_{LP}, and C_{LN}, use a B characteristic (JIS Standards) or X7R/X5R (EIA Standards), and use a ceramic capacitor with minimal reduction of capacitance when a DC bias is applied.

・ Coil, Schottky diode, P-ch MOSFET

L_P, L_N	: 3.3μH (VLF5014S-3R3M2R0, TDK-EPC) (MSS5121-332, Coilcraft)
SBD_P, SBD_N	: XBS304S17R-G (TOREX) CMS03 (TOSHIBA)
P-ch MOS	: EMH1303 (SANYO)

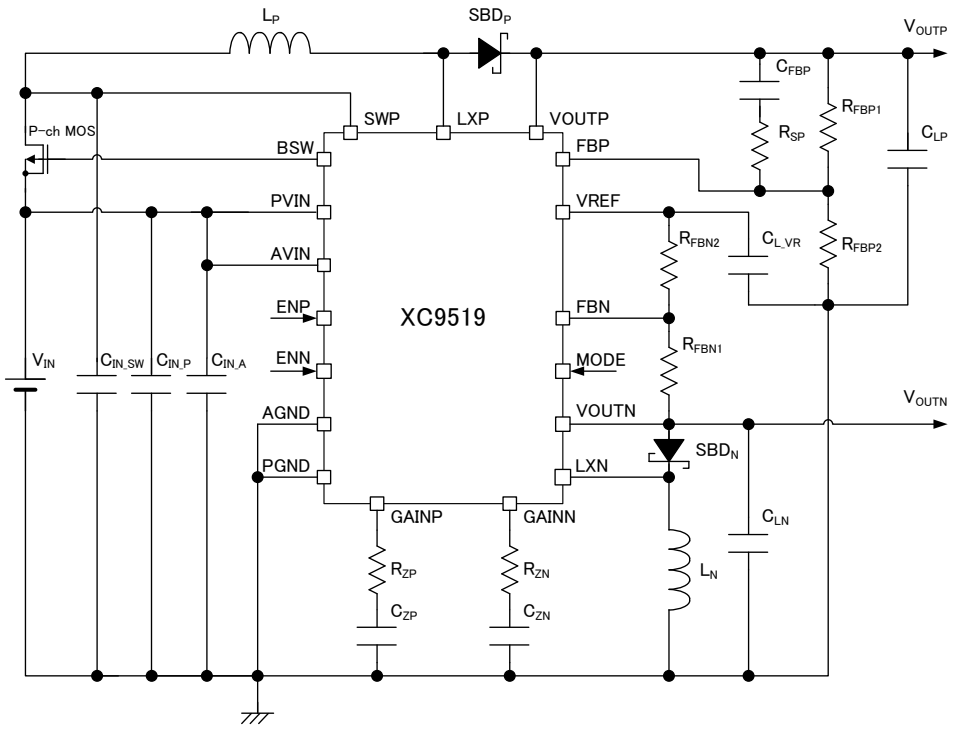
When selecting external components, refer to the specifications of each component and select so as not to exceed the ratings.

・Resistor

R_{FBP1}	: 300kΩ	R_{FBN1}	: 300kΩ	R_{ZP}	: 8.2kΩ
R_{FBP2}	: 75kΩ	R_{FBN2}	: 60kΩ	R_{ZN}	: 110kΩ
R_{SP}	: 4.7kΩ				

■TYPICAL APPLICATION CIRCUIT (Continued)

(V_{IN}=3.6V, V_{OUTP}=15.0V, V_{OUTN}=-15.0V)



<Typical Examples> V_{IN}=3.6V, V_{OUTP}=15.0V, V_{OUTN}=-15.0V

・Capacitor

C_{IN_P}	: 10μF/ 10V (C2012JB1A106M, TDK-EPC)
C_{IN_SW}	: 4.7μF/ 10V (C2012JB1A475M, TDK-EPC)
C_{IN_A}	: 0.1μF/ 10V (C1005JB1A104K, TDK-EPC)
C_{LP}	: 4×4.7μF/ 25V (TMK212BJ475KG, TAIYO YUDEN)
C_{LN}	: 4×4.7μF/ 25V (TMK212BJ475KG, TAIYO YUDEN)
C_{L_VR}	: 0.22μF/ 6.3V (C1005JB0J224M, TDK-EPC)
C_{ZP}	: 2.2nF/ 50V (C1005JB1H222K, TDK-EPC)
C_{ZN}	: 0.47nF/ 50V (C1005JB1H471K, TDK-EPC)
C_{FBP}	: OPEN

For C_{IN_P}, C_{IN_SW}, C_{IN_A}, C_{L_VR}, C_{LP}, and C_{LN}, use a B characteristic (JIS Standards) or X7R/X5R (EIA Standards), and use a ceramic capacitor with minimal reduction of capacitance when a DC bias is applied.

・ Coil, Schottky diode, P-ch MOSFET

L_P, L_N	: 3.3μH (VLF5014S-3R3M2R0, TDK-EPC) (MSS5121-332, Coilcraft)
SBD_P, SBD_N	: XBS304S17R-G (TOREX) CMS03 (TOSHIBA)
P-ch MOS	: EMH1303 (SANYO)

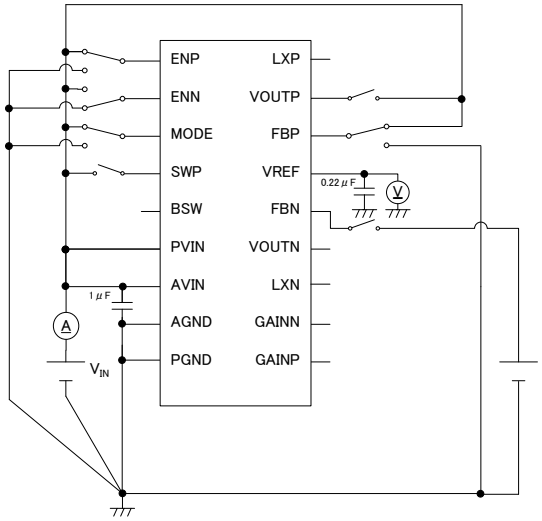
When selecting external components, refer to the specifications of each component and select so as not to exceed the ratings.

・Resistor

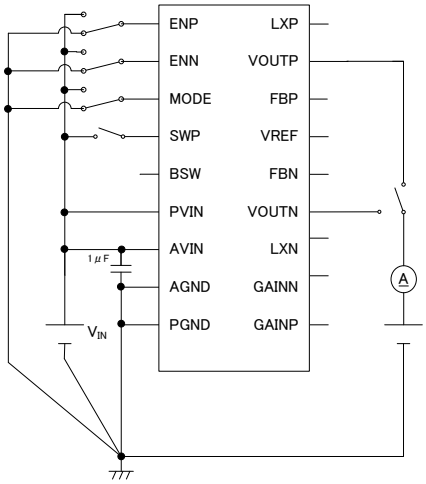
R_{FBP1}	: 336kΩ	R_{FBN1}	: 360kΩ	R_{ZP}	: 27kΩ
R_{FBP2}	: 24kΩ	R_{FBN2}	: 24kΩ	R_{ZN}	: 200kΩ
R_{SP}	: OPEN				

■TEST CIRCUITS

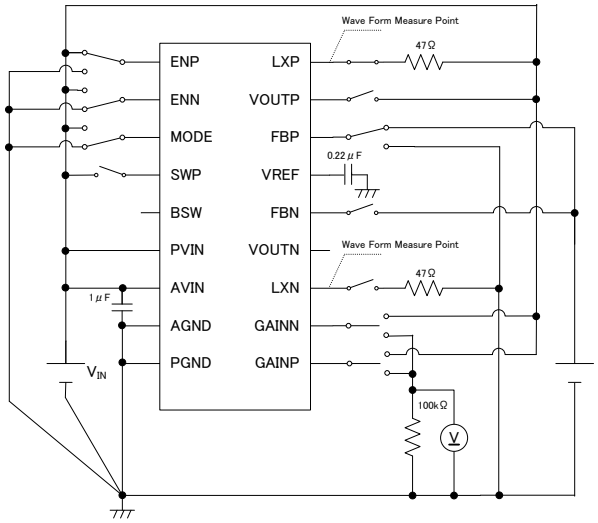
1) Circuit ①



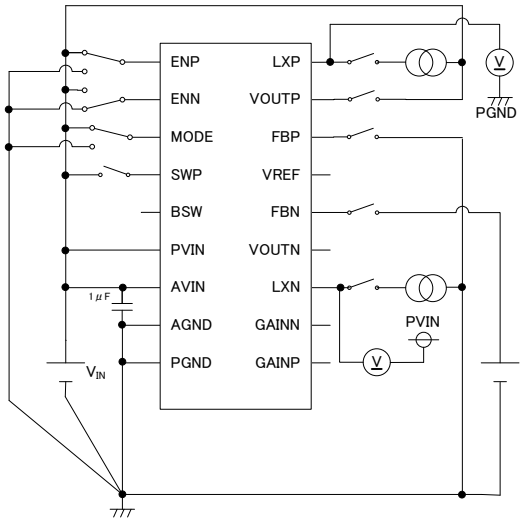
2) Circuit ②



3) Circuit ③

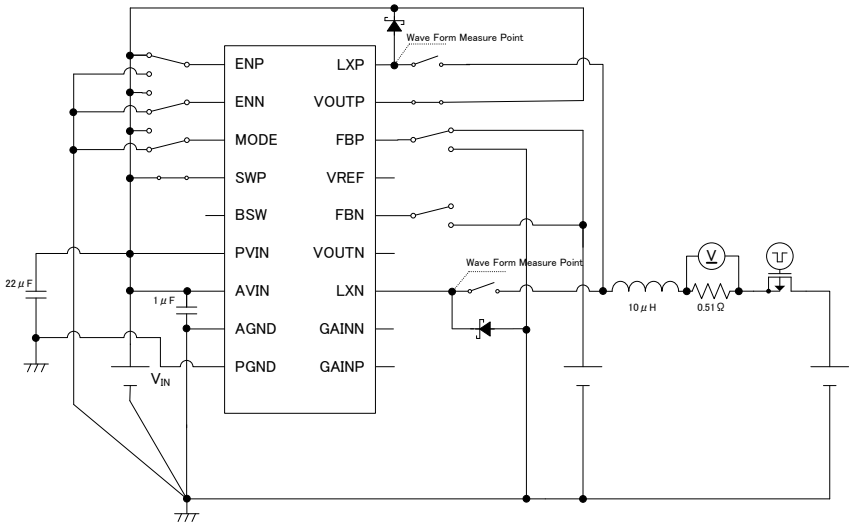


4) Circuit ④

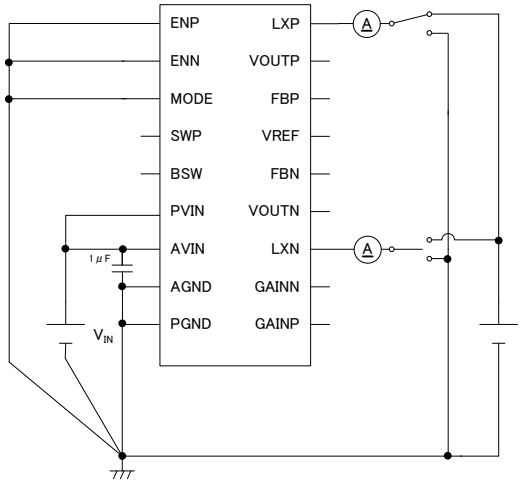


■TEST CIRCUITS (Continued)

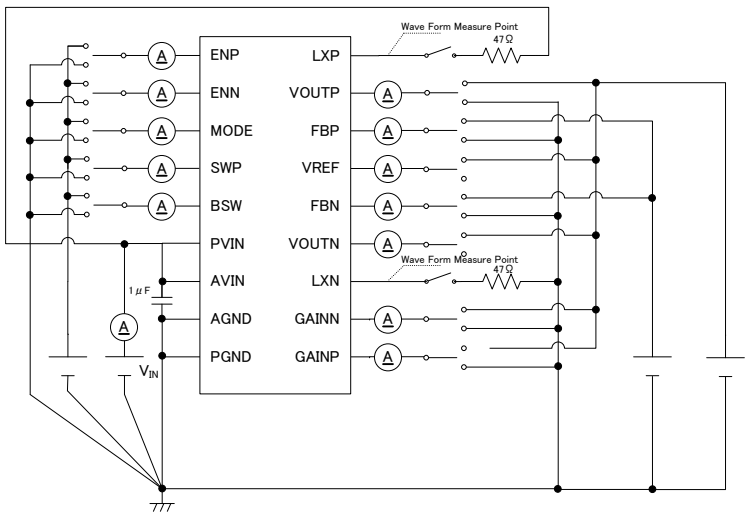
5) Circuit ⑤



6) Circuit ⑥

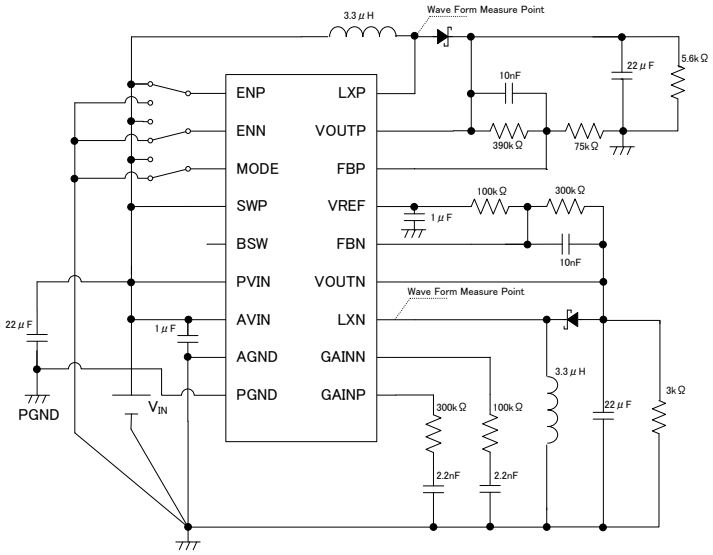


7) Circuit ⑦

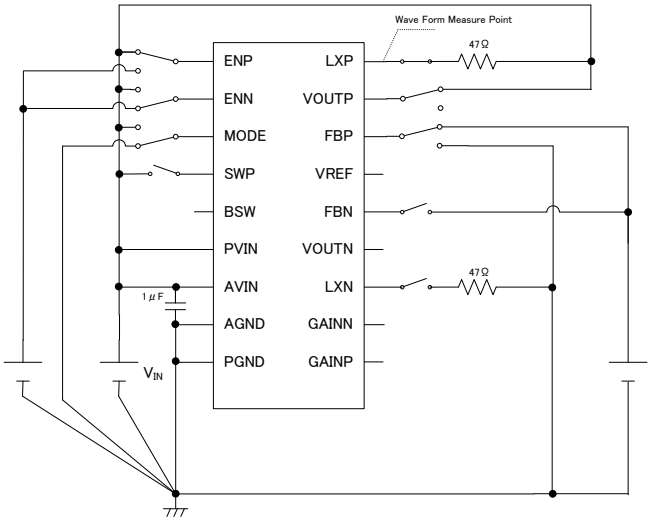


■TEST CIRCUITS (Continued)

8) Circuit ⑧



9) Circuit ⑨



1. Capacitance between pins

The capacitances between the following pins are omitted in the circuit diagram.

PVIN pin – PGND pin: 1μF

FBP pin - AGND pin: 1μF

FBN pin - AGND pin: 1μF

VREF pin - AGND pin: 1μF

2. Testing method for on resistance

Testing is executed at 100% DUTY using test mode.

■NOTES ON USE

1. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

2. The characteristics of this IC are highly dependent on peripheral circuits.
   When selecting external components, refer to the specifications of each component and select so as not to exceed the ratings.
   Some peripheral component selections may cause unstable operation.
   Before use, sufficiently test operation using the actual equipment.

3. When the input voltage V_{IN} is low and the output voltage V_{OUTP}/V_{OUTN} is high, the input current may be limited by the maximum duty limit and the set output voltage may not be output.

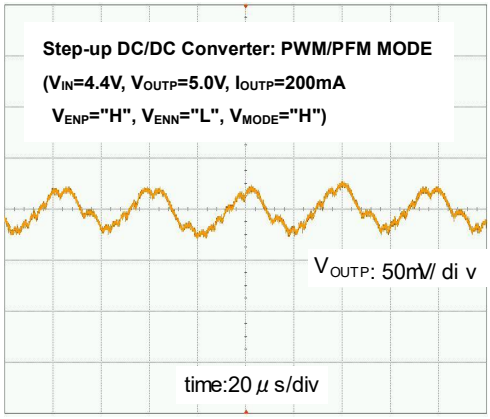
4. If the step-up ratio is high and excessive load current flows, the input current may be limited by the maximum duty limit and maximum current limit protection and short-circuit protection may not activate.

5. Do not connect a component other than C_{L_VR} to the VREF pin.
   If a component other than C_{L_VR} is connected, the output voltage V_{OUTN} of an inverting DC/DC converter may become unstable.

6. For external components, use the components specified in the standard circuit examples and component selection methods.

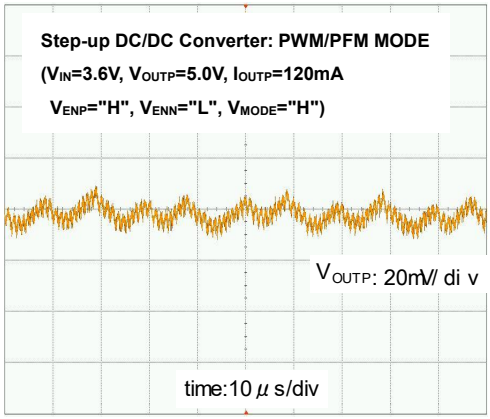
7. When the input voltage V_{IN} is high and the output voltage V_{OUTP}/V_{OUTN} is low, intermittent oscillation may occur during PWM control.

8. If the step-up ratio is low in a step-up DC/DC converter, the output voltage V_{OUTP} may become unstable during PFM/PWM switching control (V_{MODE} = "H").



<External Components>
C_{LP}=4×4.7 μF
L_P=3.3 μH (VLF5014S-3R3M2R0)
SBD_P: CMS03
P-ch MOS: EMH1303
R_{ZP}=7.5kΩ, C_{ZP}=4.7nF

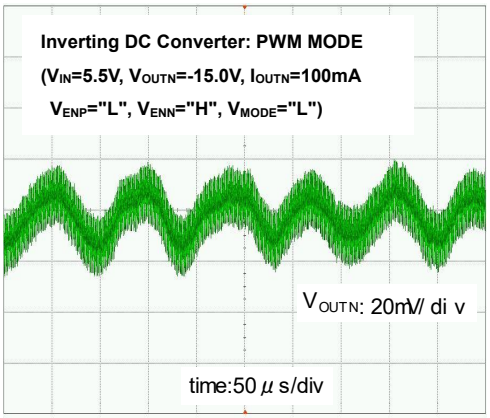
9. During PFM/PWM switching control (V_{MODE} = "H"), the output voltage may become unstable near switching between PFM mode and PWM mode.



<External Components>
C_{LP}=4×4.7 μF
L_P=3.3 μH (VLF5014S-3R3M2R0)
SBD_P: CMS03
P-ch MOS: EMH1303
R_{ZP}=7.5kΩ, C_{ZP}=4.7nF

■NOTES ON USE (Continued)

10. During PWM control (V_{MODE} = "L"), the output voltage may become unstable at light loads.



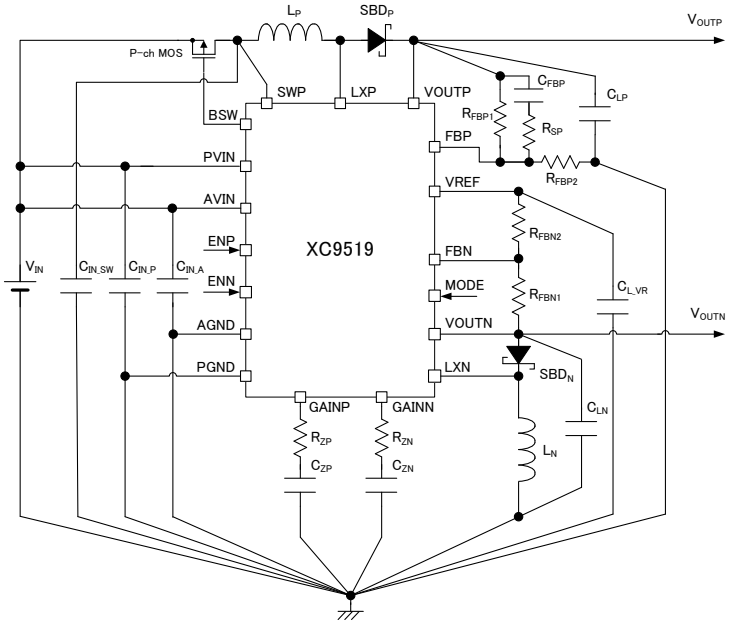
<External Components>
C_{LN}=4×4.7μF
L_N=3.3μH (VLF5014S-3R3M2R0)
SBD_N: CMS03
R_{ZN}=200kΩ, C_{ZN}=0.47nF

11. Torex places an importance on improving our products and their reliability.
We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

■NOTES ON USE (Continued)

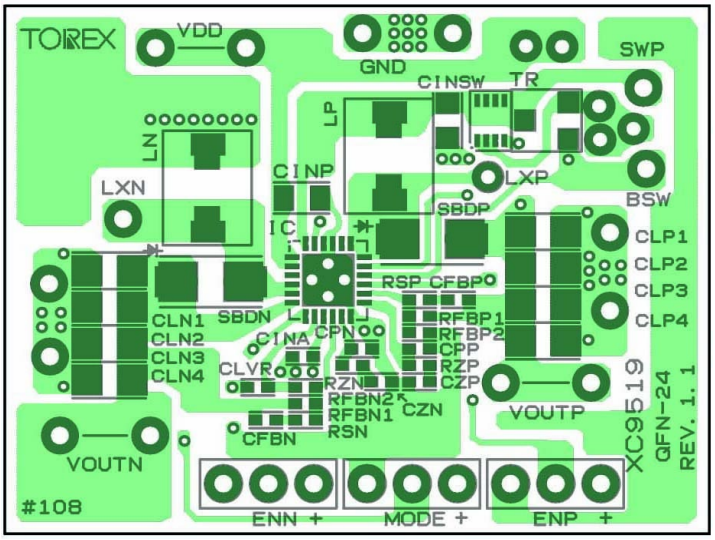
●Notes on Layout

1. Position external components close to the IC so that the wiring is thick and short.
2. To minimize input voltage fluctuations, place C_{IN_P} and C_{IN_A} as close as possible to the IC.
3. Make the GND wiring sufficiently strong. Fluctuations of AGND or PGND voltage due to GND current during switching may cause unstable IC operation.
4. When creating a layout, refer to the circuit diagram and recommended layout pattern below.
5. This product is incorporated into a driver, and thus the driver transistor current and on-resistance may cause heat generation.

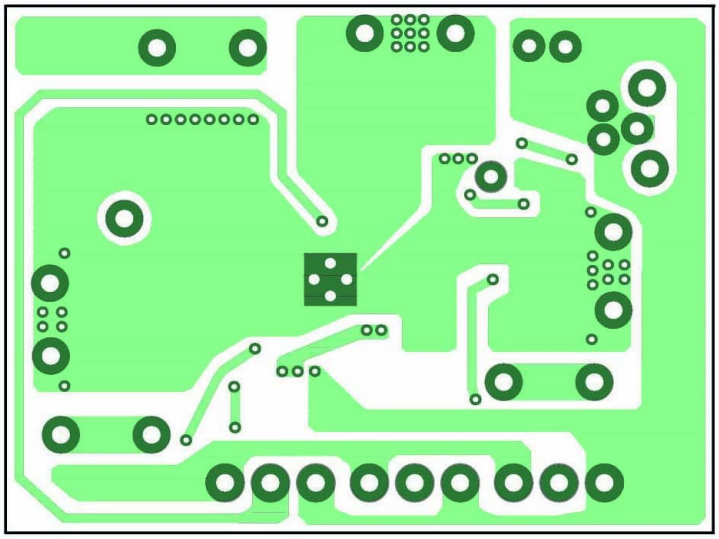


●Recommended Pattern Layout

Front



Back side see-through



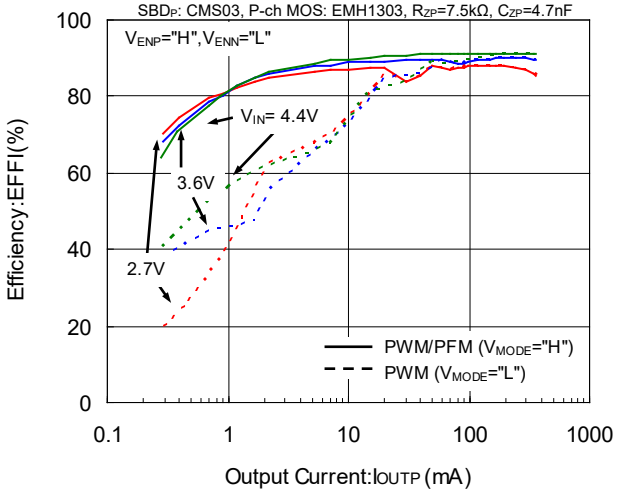
■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Efficiency vs. Output Current

Step-up DC/DC Converter (V_{OUTP}=5.0V)

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0)

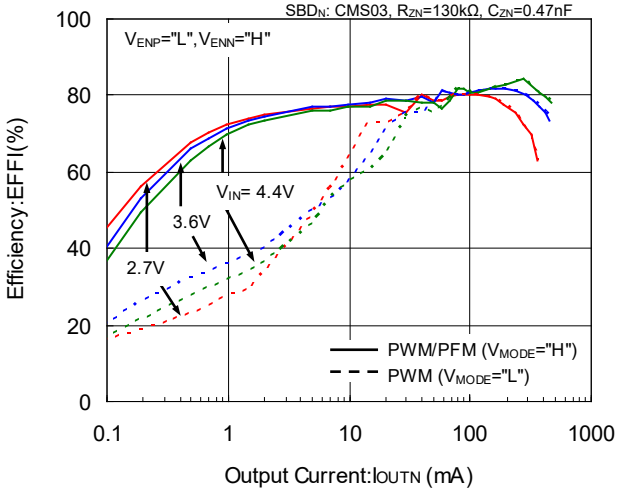
SBD_P: CMS03, P-ch MOS: EMH1303, R_{ZP}=7.5kΩ, C_{ZP}=4.7nF



Inverting DC/DC Converter (V_{OUTN}=-5.0V)

C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

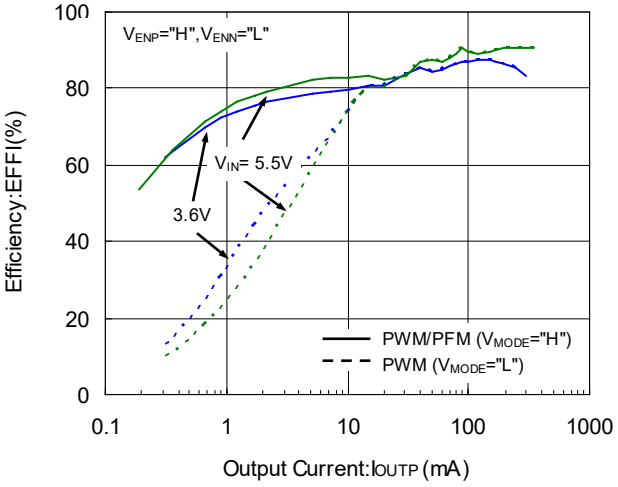
SBD_N: CMS03, R_{ZN}=130kΩ, C_{ZN}=0.47nF



Step-up DC/DC Converter

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0)

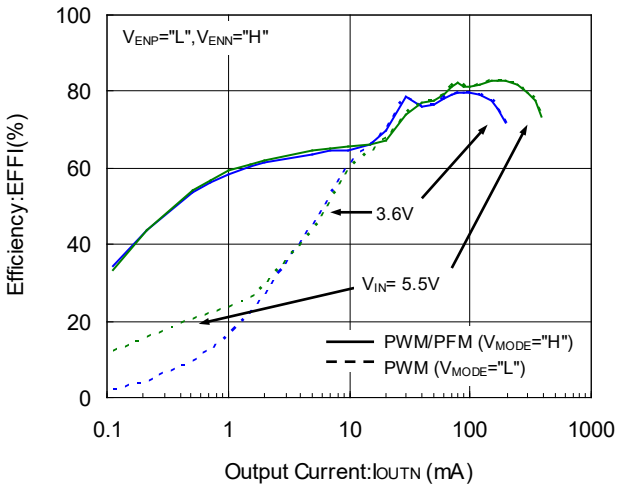
SBD_P: CMS03, P-ch MOS: EMH1303, R_{ZP}=27kΩ, C_{ZP}=2.2nF



Inverting DC/DC Converter (V_{OUTN}=-15.0V)

C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

SBD_N: CMS03, R_{ZN}=200kΩ, C_{ZN}=0.47nF

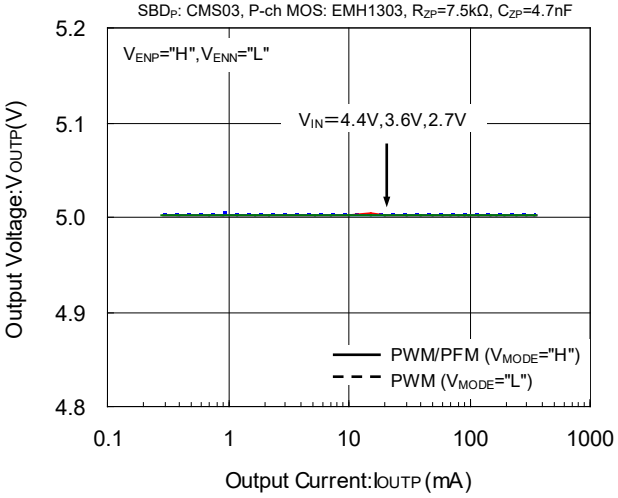


(2) Output Voltage vs. Output Current

Step-up DC/DC Converter (V_{OUTP}=5.0V)

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0)

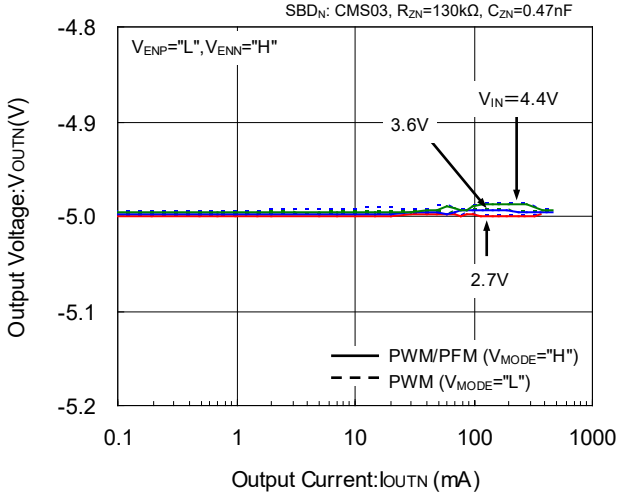
SBD_P: CMS03, P-ch MOS: EMH1303, R_{ZP}=7.5kΩ, C_{ZP}=4.7nF



Inverting DC/DC Converter (V_{OUTN}=-5.0V)

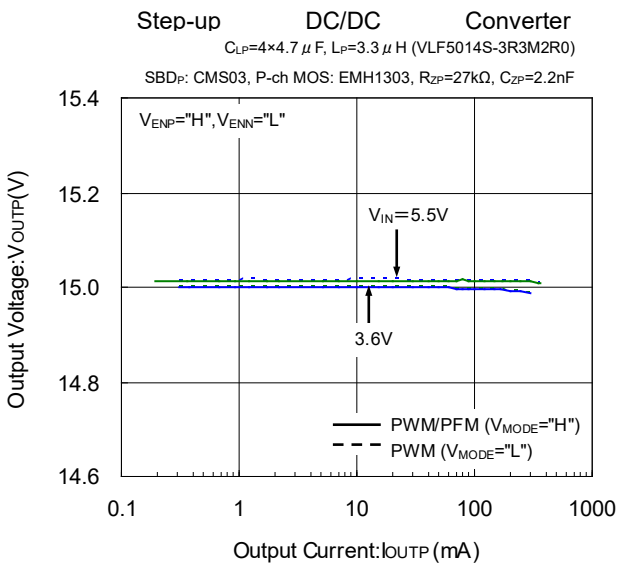
C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

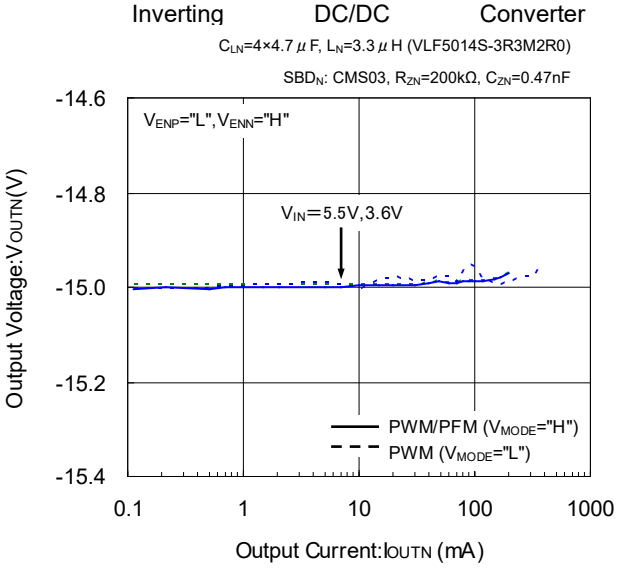
SBD_N: CMS03, R_{ZN}=130kΩ, C_{ZN}=0.47nF



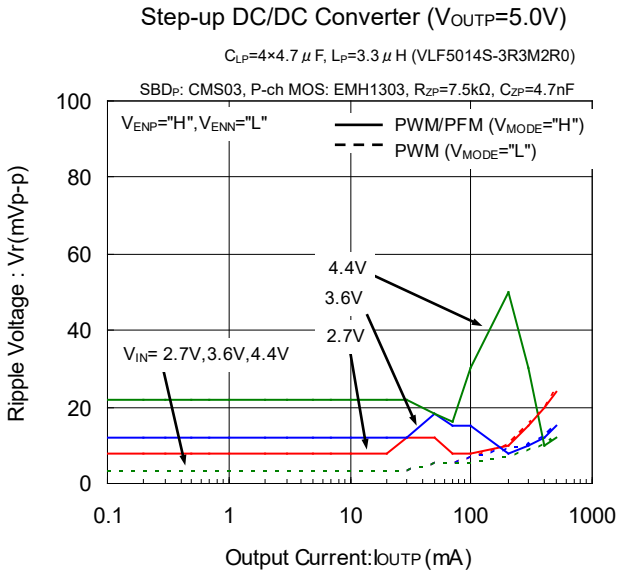
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

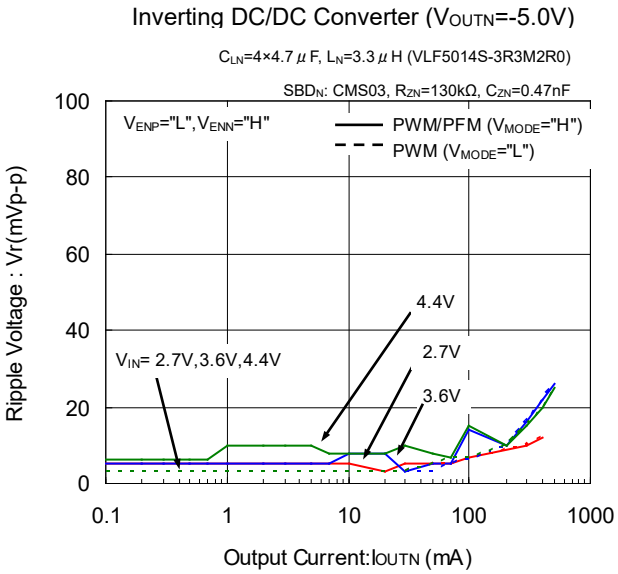
(2) Output Voltage vs. Output Current (Continued)

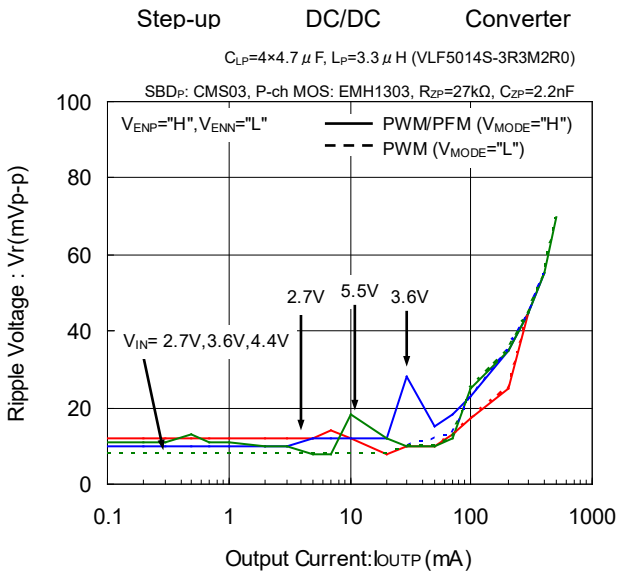


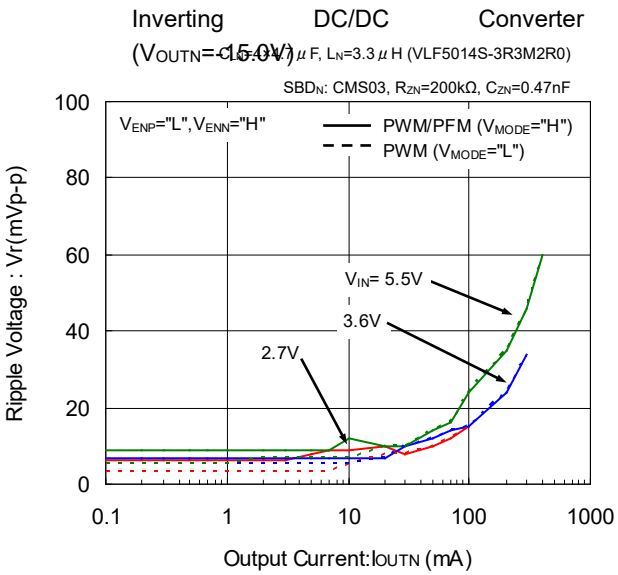


(3) Ripple Voltage vs. Output Current



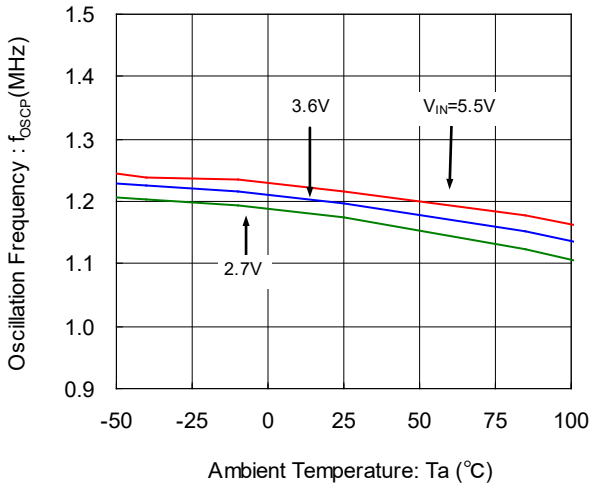


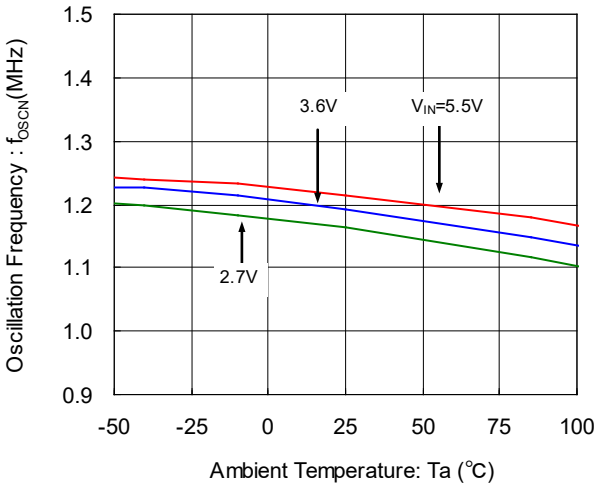




■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

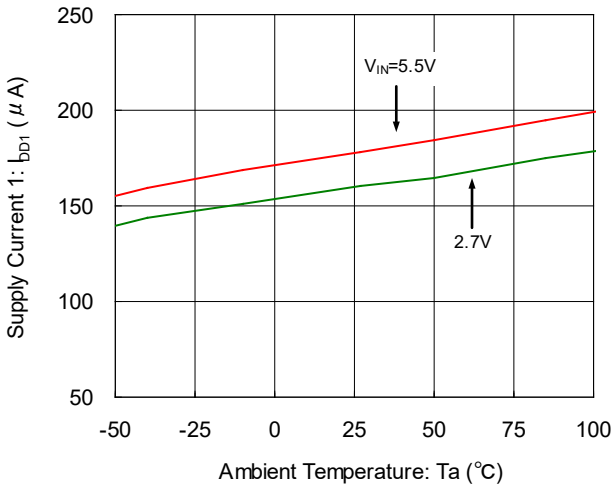
(4) Oscillation Frequency vs. Ambient Temperature



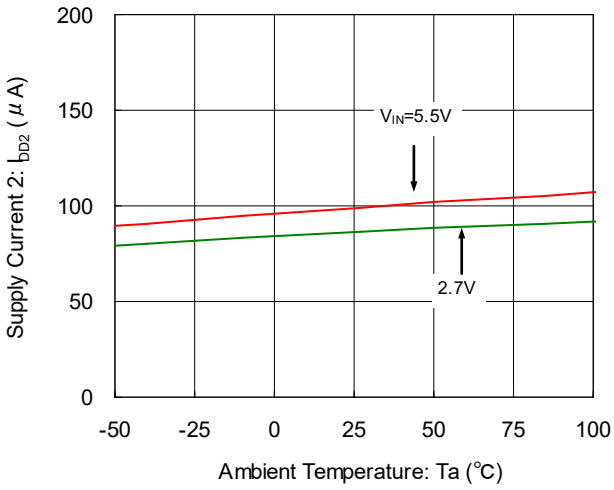


(5) Supply Current 1,2,3 vs. Ambient Temperature

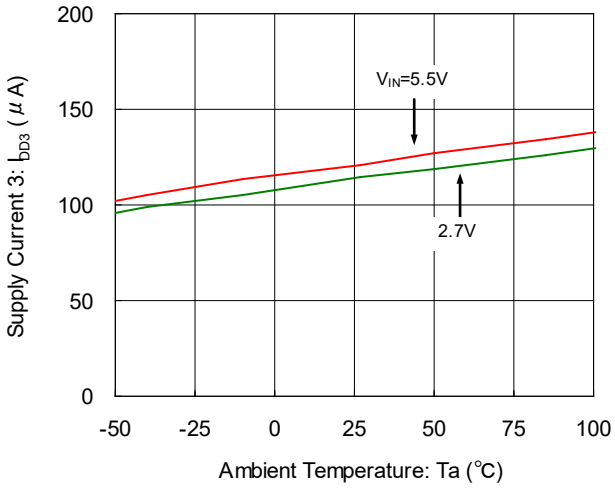
Supply Current 1



Supply Current 2

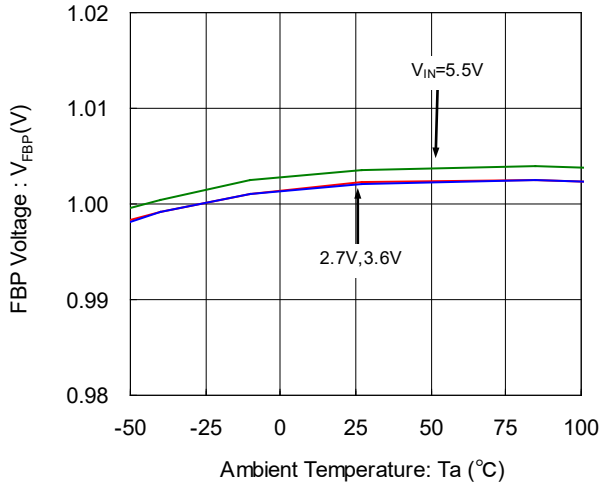


Supply Current 3

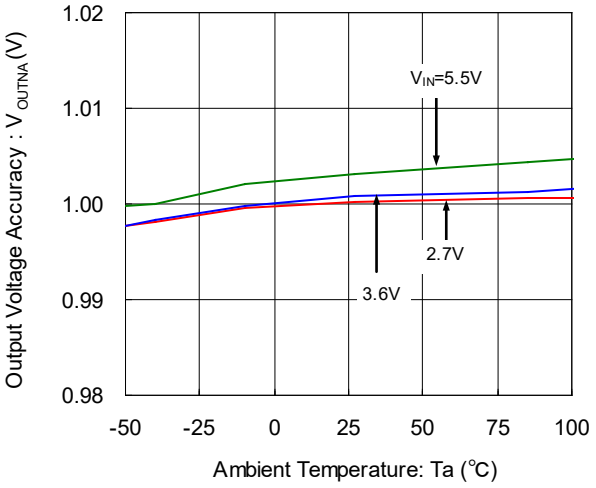


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

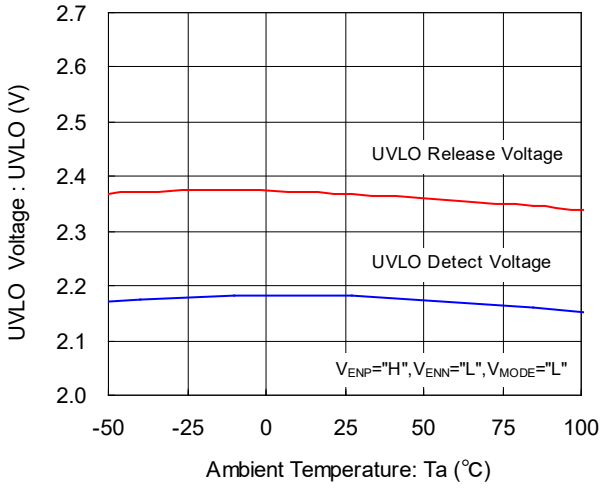
(6) FBP Voltage vs. Ambient Temperature



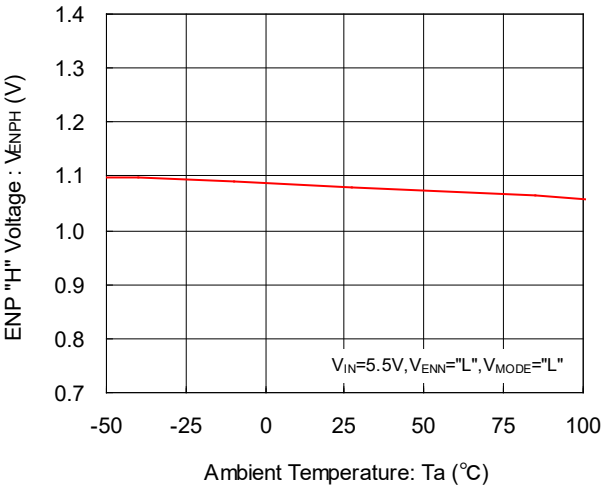
(7) Output Voltage Accuracy vs. Ambient Temperature



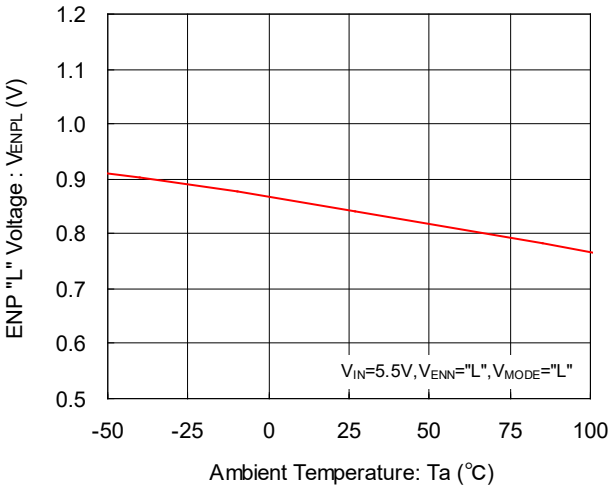
(8) UVLO Voltage vs. Ambient Temperature



(9) ENP "H" Voltage vs. Ambient Temperature

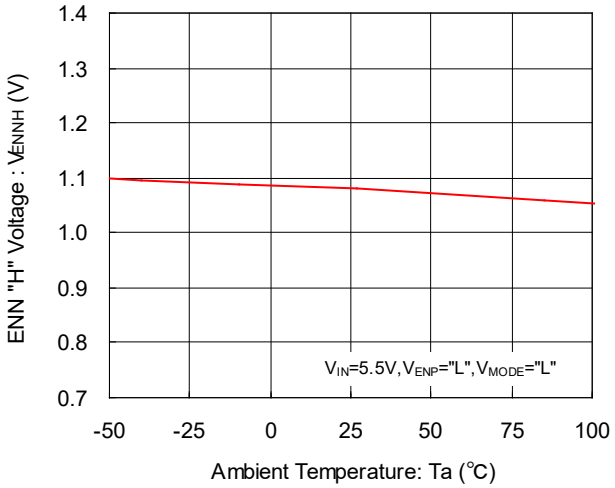


(10) ENP "L" Voltage vs. Ambient Temperature

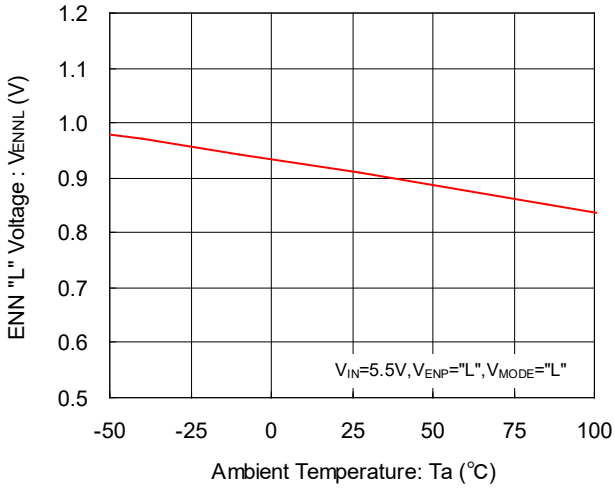


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

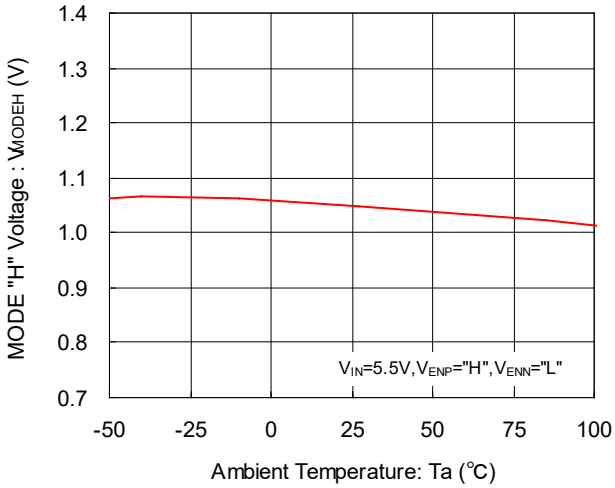
(11) ENN "H" Voltage vs. Ambient Temperature



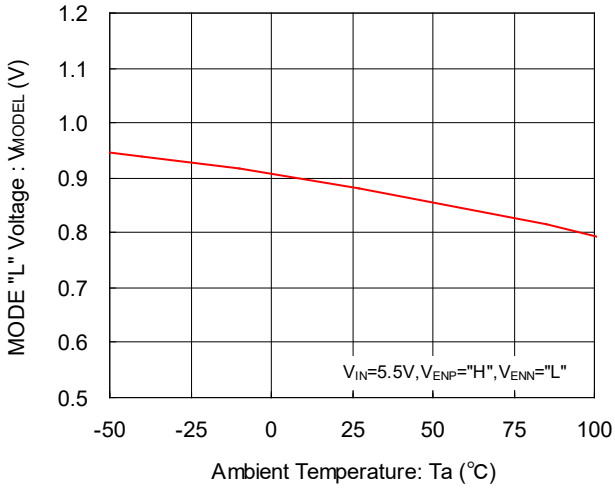
(12) ENN "L" Voltage vs. Ambient Temperature



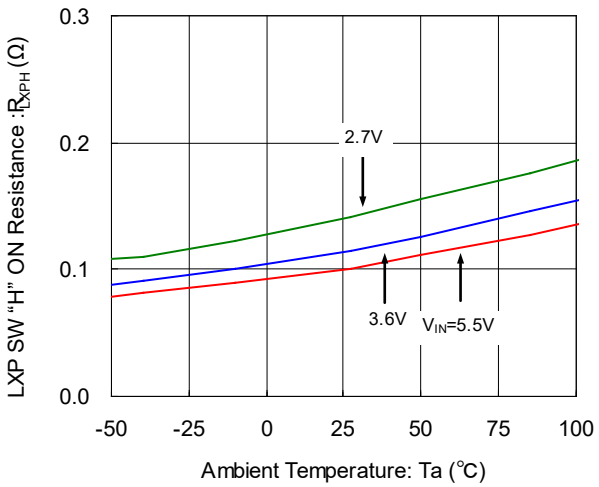
(13) MODE "H" Voltage vs. Ambient Temperature



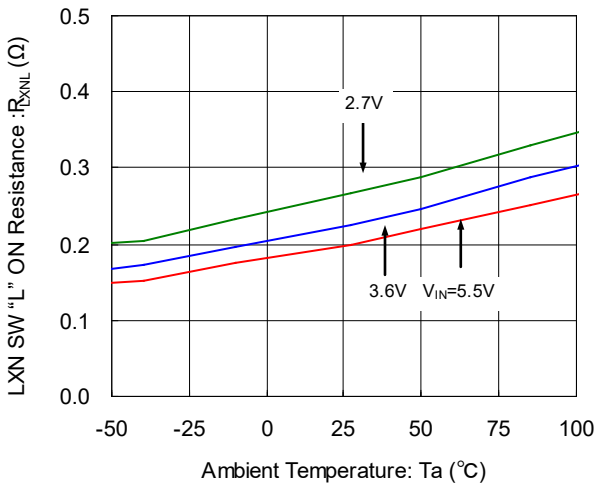
(14) MODE "L" Voltage vs. Ambient Temperature



(15) LXP SW “H” ON Resistance vs. Ambient Temperature



(16) LXN SW "L" ON Resistance vs. Ambient Temperature



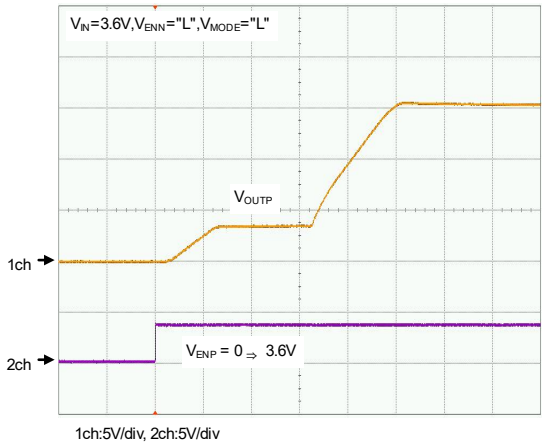
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(17) Output Voltage Rise Wave Form

Step-up DC/DC Converter

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0)

SBD_P: CMS03, P-ch MOS: EMH1303, R_{ZP}=27kΩ, C_{ZP}=2.2nF

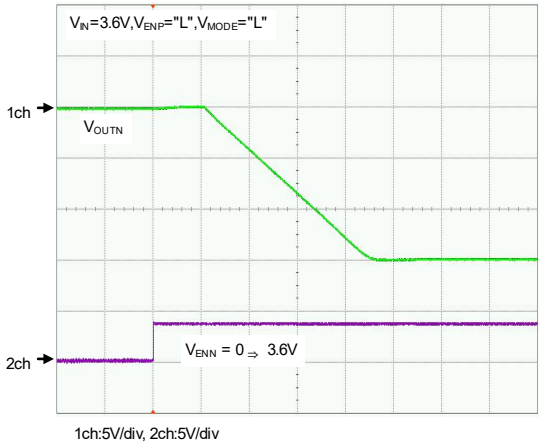


time:500μs/div

Inverting DC/DC Converter (V_{OUTN}=-15.0V)

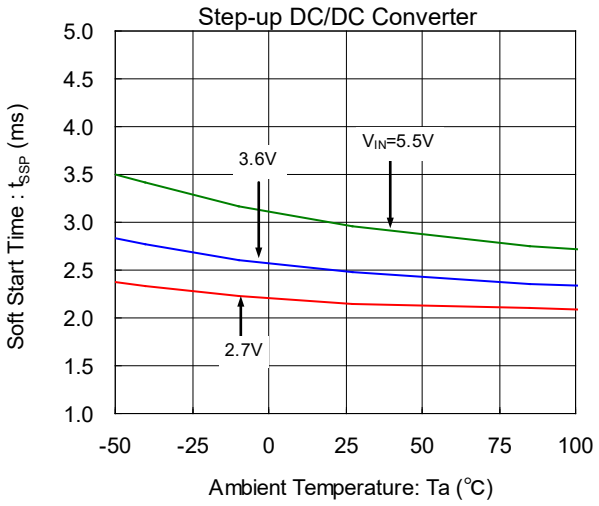
C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

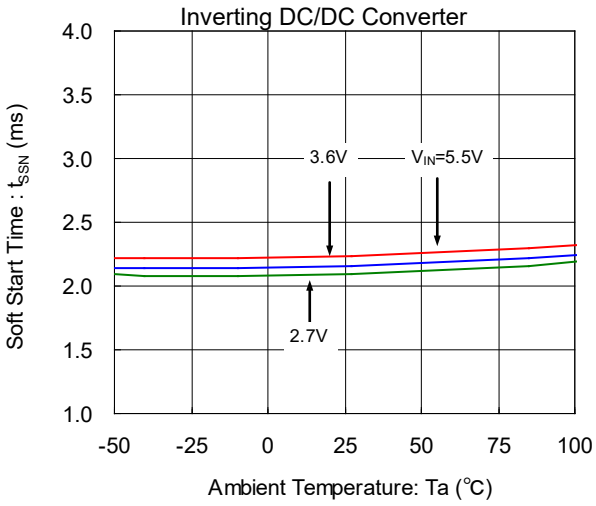
SBD_N: CMS03, R_{ZN}=200kΩ, C_{ZN}=0.47nF



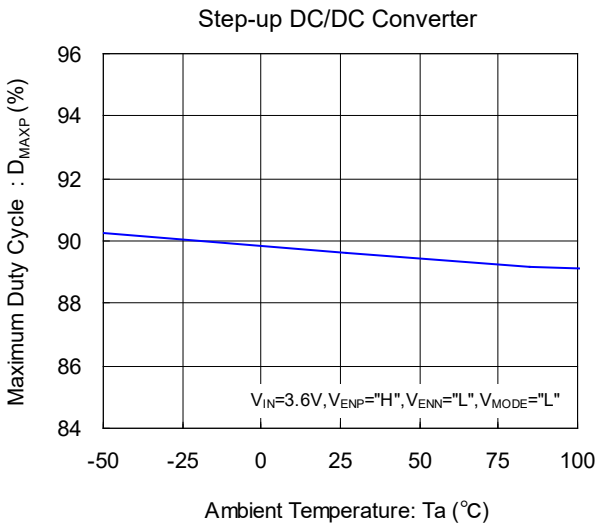
time:500μs/div

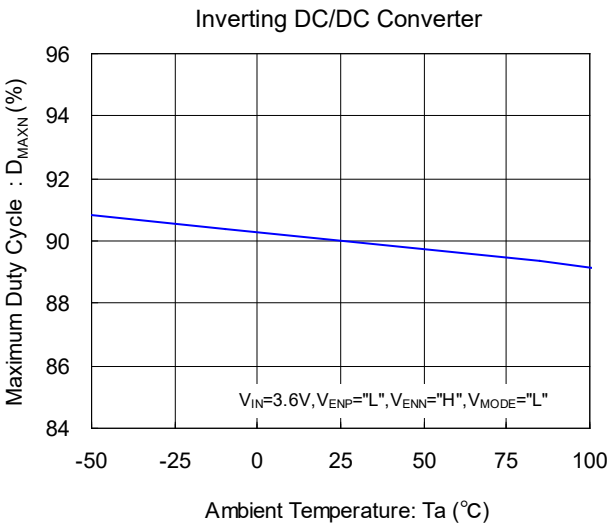
(18) Soft Start Time vs. Ambient Temperature





(19) Maximum Duty Cycle vs. Ambient Temperature





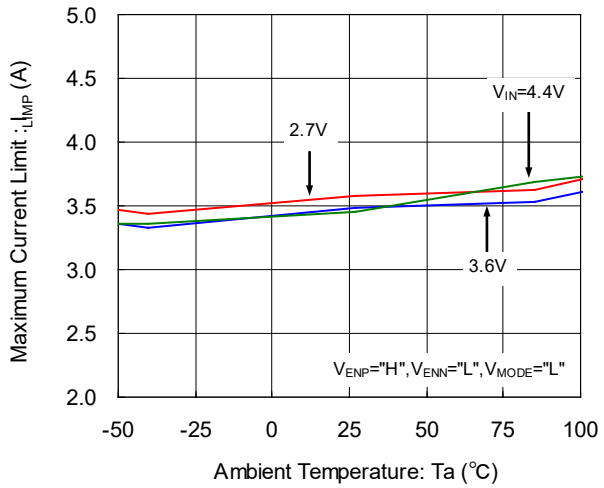
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(20) Maximum Current Limit vs. Ambient Temperature

Step-up DC/DC Converter (V_{OUTP}=5.0V)

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0)

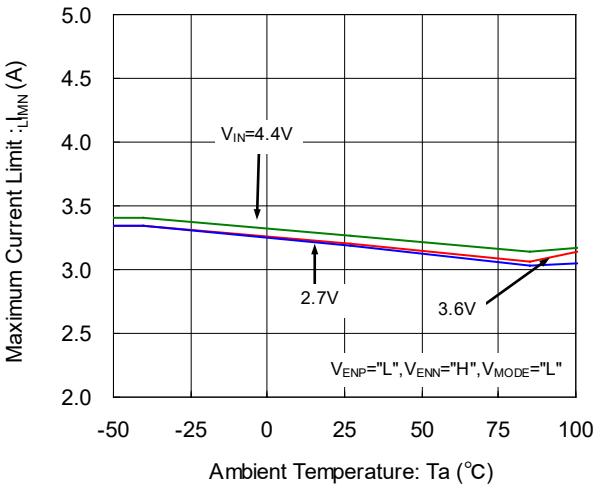
SBD_P: CMS03, P-ch MOS: EMH1303, R_{ZP}=7.5kΩ, C_{ZP}=4.7nF



Inverting DC/DC Converter (V_{OUTN}=-5.0V)

C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

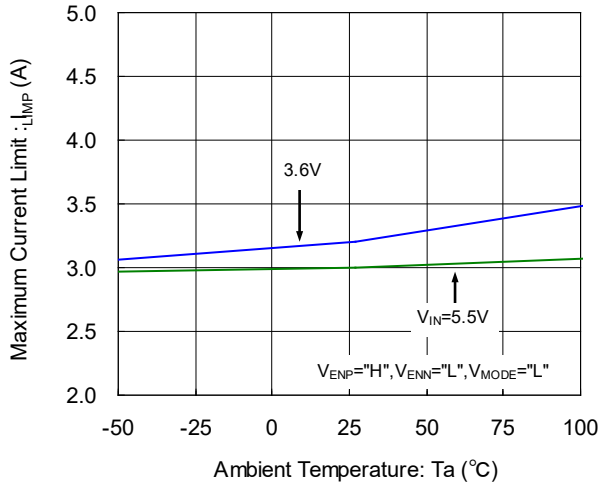
SBD_N: CMS03, R_{ZN}=130kΩ, C_{ZN}=0.47nF



Step-up DC/DC Converter (V_{OUTP}=15.0V)

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0)

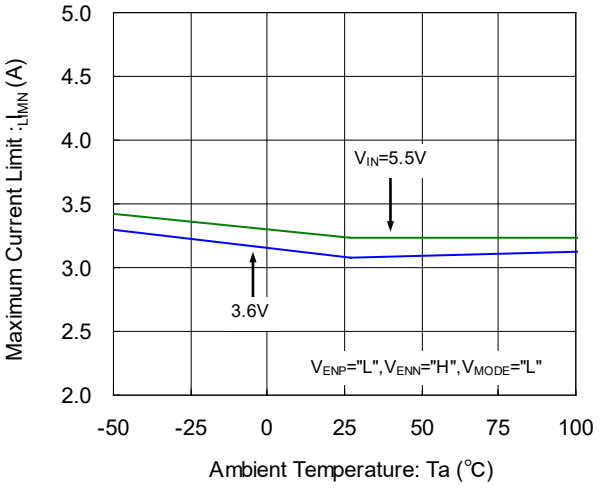
SBD_P: CMS03, P-ch MOS: EMH1303, R_{ZP}=27kΩ, C_{ZP}=2.2nF



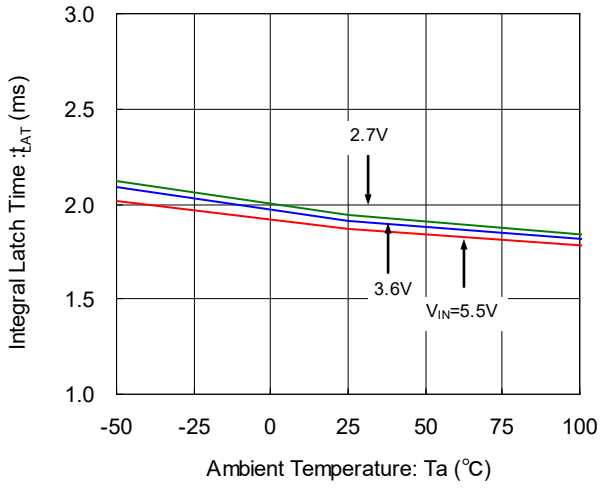
Inverting DC/DC Converter (V_{OUTN}=-15.0V)

C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

SBD_N: CMS03, R_{ZN}=200kΩ, C_{ZN}=0.47nF

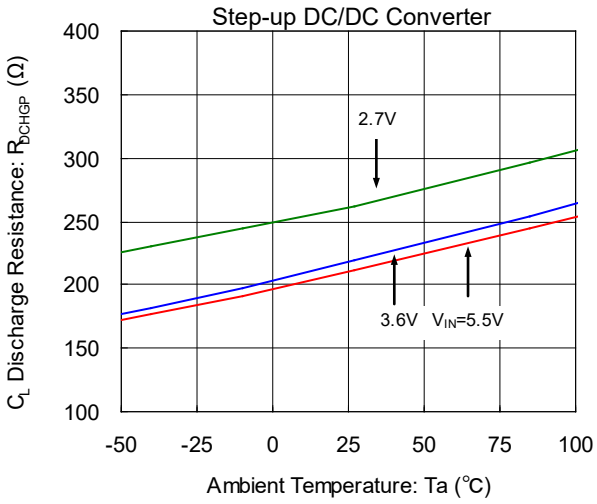


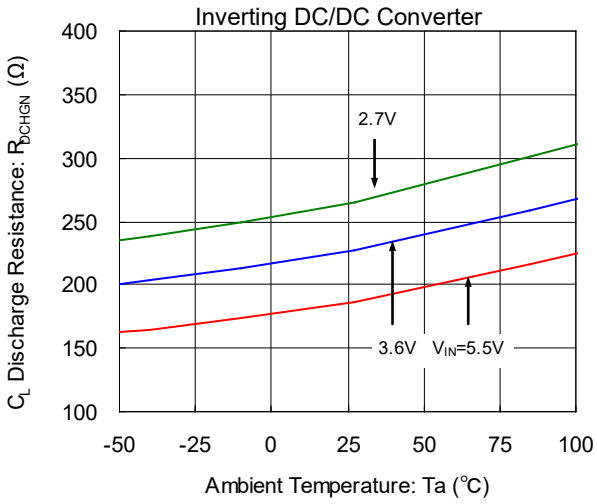
(21) Latch Time vs. Ambient Temperature



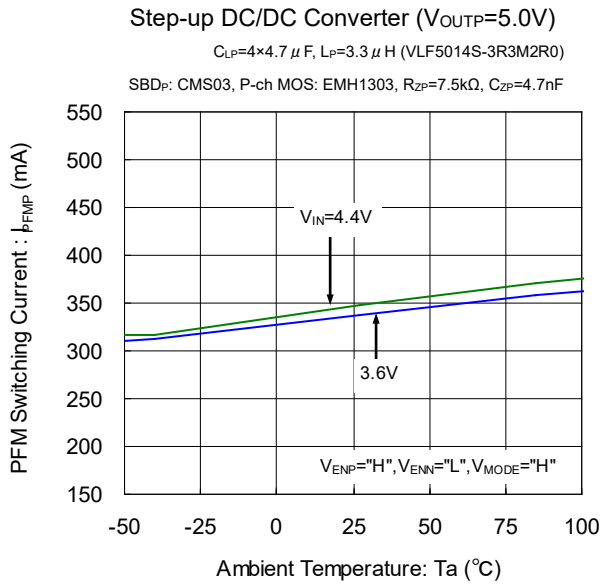
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

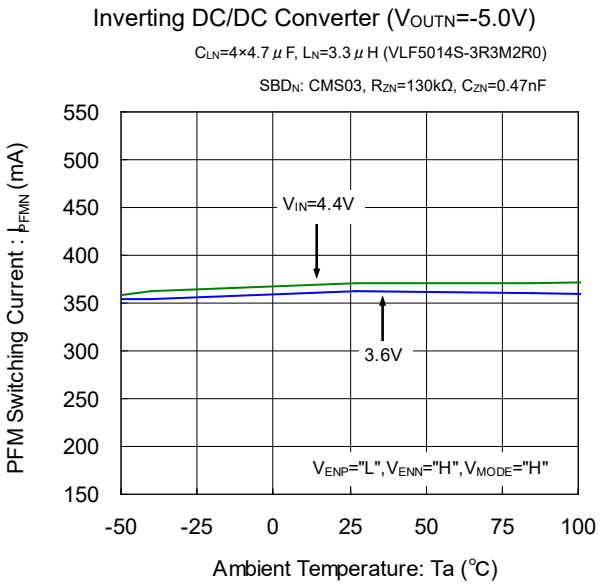
(22) C_L Discharge Resistance vs. Ambient Temperature

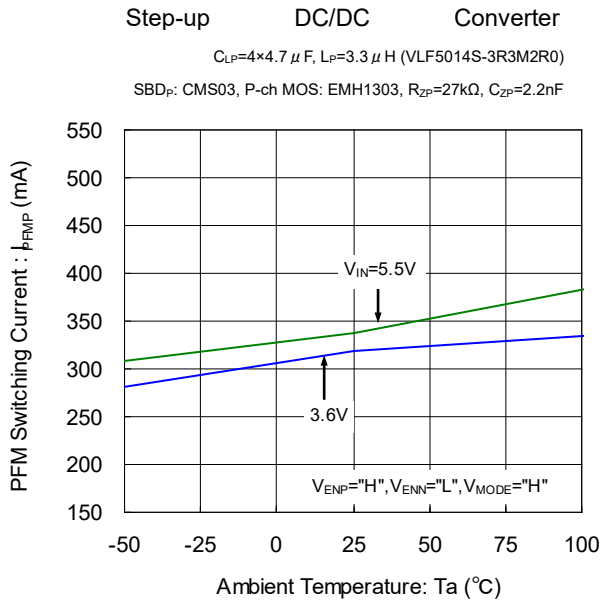


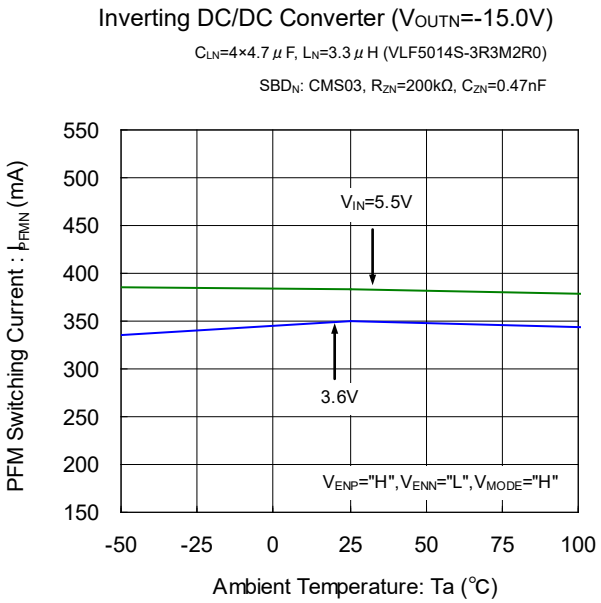


(23) PFM Switching Current vs. Ambient Temperature







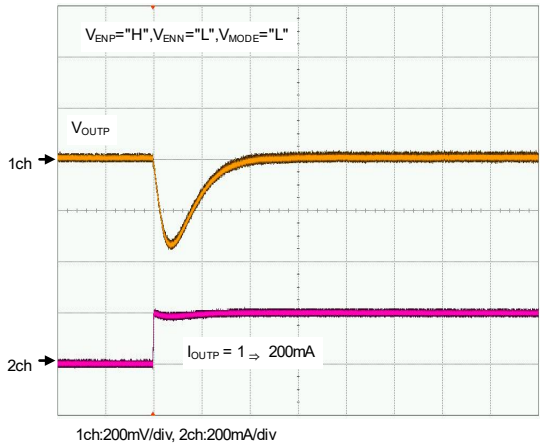


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(24) Load Transient Response

Step-up DC/DC Converter: PWM/PFM MODE
(V_{IN}=3.6V, V_{OUTP}=5.0V, I_{OUTP}=1⇒200mA)

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0), SBD_P: CMS03
P-ch MOS: EMH1303, R_{ZP}=8.2kΩ, C_{ZP}=4.7nF, C_{FBP}=47pF, R_{SP}=4.7kΩ

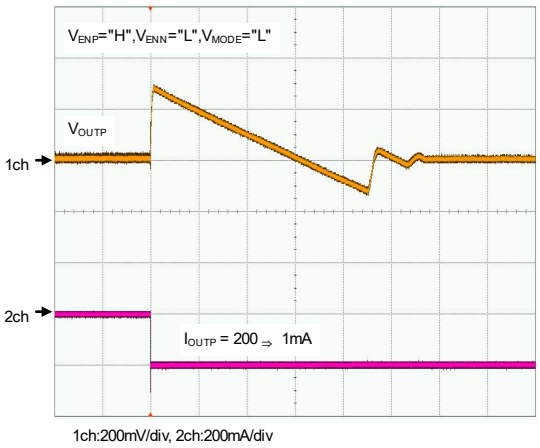


1ch:200mV/div, 2ch:200mA/div

time:100μs/div

Step-up DC/DC Converter: PWM MODE
(V_{IN}=3.6V, V_{OUTP}=5.0V, I_{OUTP}=200⇒1mA)

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0), SBD_P: CMS03
P-ch MOS: EMH1303, R_{ZP}=8.2kΩ, C_{ZP}=4.7nF, C_{FBP}=47pF, R_{SP}=4.7kΩ

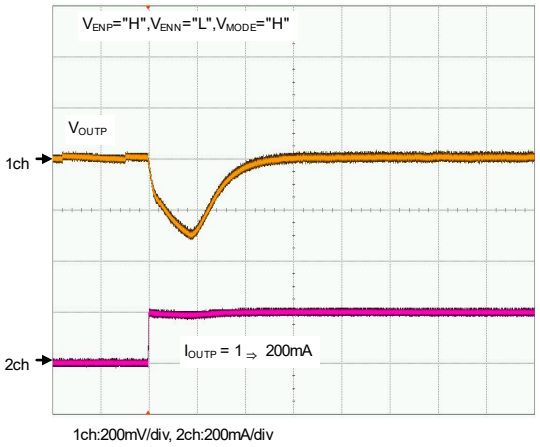


1ch:200mV/div, 2ch:200mA/div

time:1ms/div

Step-up DC/DC Converter: PWM/PFM MODE
(V_{IN}=3.6V, V_{OUTP}=5.0V, I_{OUTP}=1⇒200mA)

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0), SBD_P: CMS03
P-ch MOS: EMH1303, R_{ZP}=8.2kΩ, C_{ZP}=4.7nF, C_{FBP}=47pF, R_{SP}=4.7kΩ

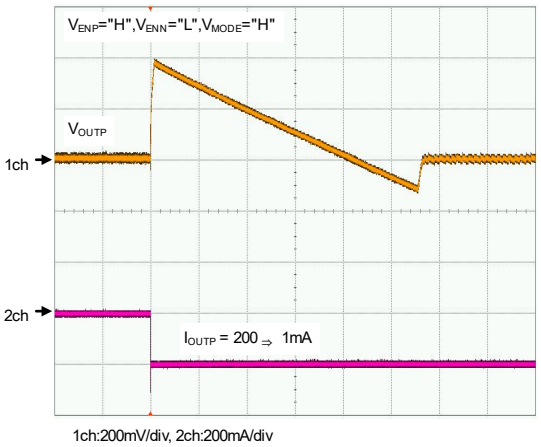


1ch:200mV/div, 2ch:200mA/div

time:100μs/div

Step-up DC/DC Converter: PWM/PFM MODE
(V_{IN}=3.6V, V_{OUTP}=5.0V, I_{OUTP}=200⇒1mA)

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0), SBD_P: CMS03
P-ch MOS: EMH1303, R_{ZP}=8.2kΩ, C_{ZP}=4.7nF, C_{FBP}=47pF, R_{SP}=4.7kΩ



1ch:200mV/div, 2ch:200mA/div

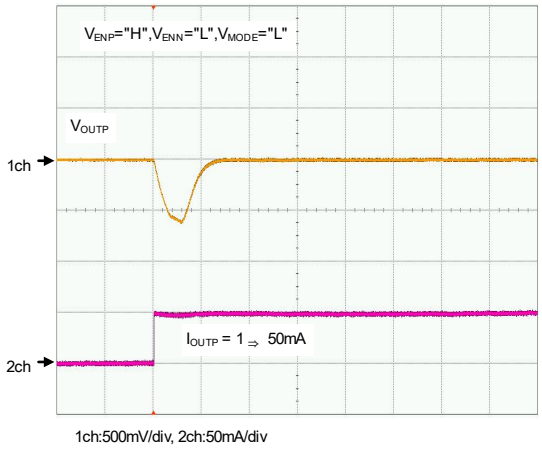
time:1ms/div

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Step-up DC/DC Converter: PWM MODE
(V_{IN}=3.6V, V_{OUTP}=15.0V, I_{OUTP}=1⇒50mA)

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0)

SBD_P: CMS03, P-ch MOS: EMH1303, R_{ZP}=27kΩ, C_{ZP}=2.2nF



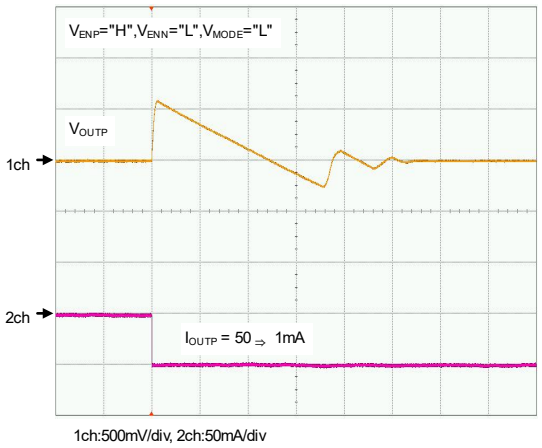
1ch:500mV/div, 2ch:50mA/div

time:200μs/div

Step-up DC/DC Converter: PWM MODE
(V_{IN}=3.6V, V_{OUTP}=15.0V, I_{OUTP}=50⇒1mA)

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0)

SBD_P: CMS03, P-ch MOS: EMH1303, R_{ZP}=27kΩ, C_{ZP}=2.2nF



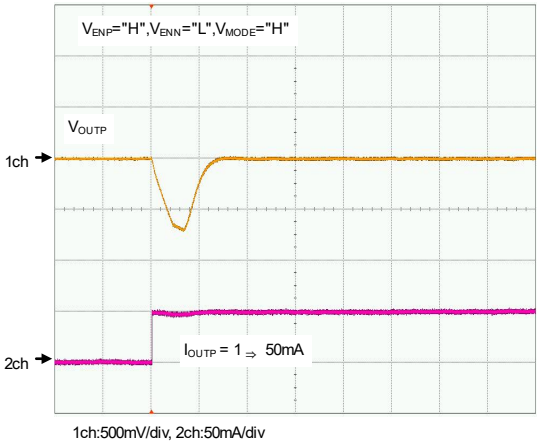
1ch:500mV/div, 2ch:50mA/div

time:1ms/div

Step-up DC/DC Converter: PWM/PFM MODE
(V_{IN}=3.6V, V_{OUTP}=15.0V, I_{OUTP}=1⇒50mA)

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0)

SBD_P: CMS03, P-ch MOS: EMH1303, R_{ZP}=27kΩ, C_{ZP}=2.2nF



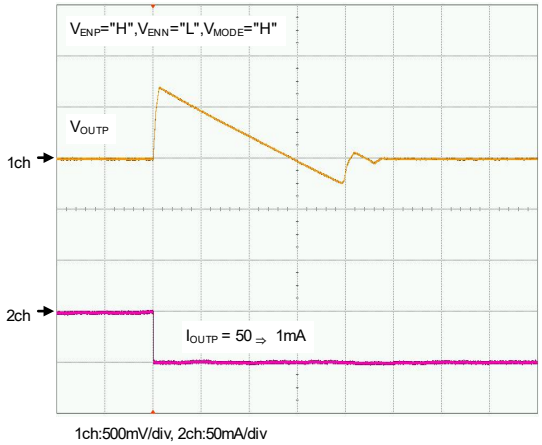
1ch:500mV/div, 2ch:50mA/div

time:200μs/div

Step-up DC/DC Converter: PWM/PFM MODE
(V_{IN}=3.6V, V_{OUTP}=15.0V, I_{OUTP}=50⇒1mA)

C_{LP}=4×4.7μF, L_P=3.3μH (VLF5014S-3R3M2R0)

SBD_P: CMS03, P-ch MOS: EMH1303, R_{ZP}=27kΩ, C_{ZP}=2.2nF



1ch:500mV/div, 2ch:50mA/div

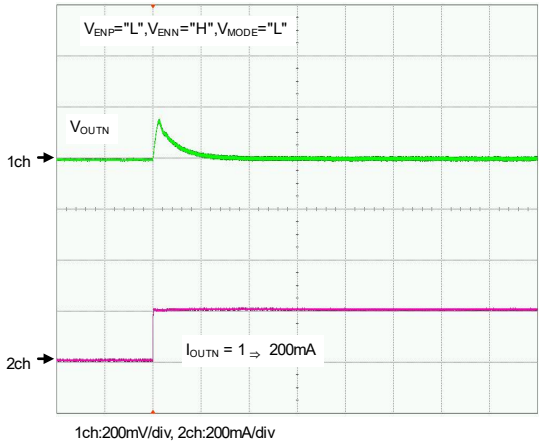
time:1ms/div

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Inverting DC/DC Converter: PWM MODE
(V_{IN}=3.6V, V_{OUTN}=-5.0V, I_{OUTN}=1⇒200mA)

C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

SBD_N: CMS03, R_{ZN}=130kΩ, C_{ZN}=0.47nF



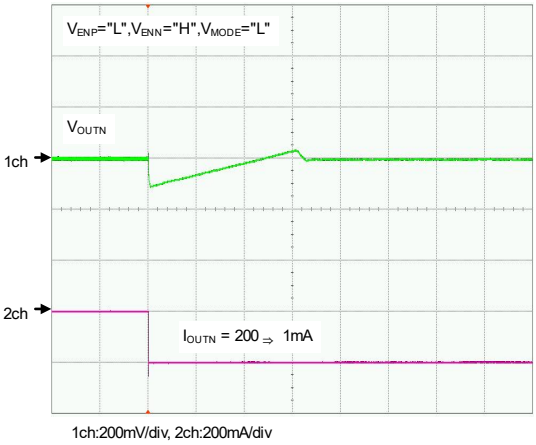
1ch:200mV/div, 2ch:200mA/div

time:100μs/div

Inverting DC/DC Converter: PWM MODE
(V_{IN}=3.6V, V_{OUTN}=-5.0V,
I_{OUTN}=200⇒1mA)

C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

SBD_N: CMS03, R_{ZN}=130kΩ, C_{ZN}=0.47nF



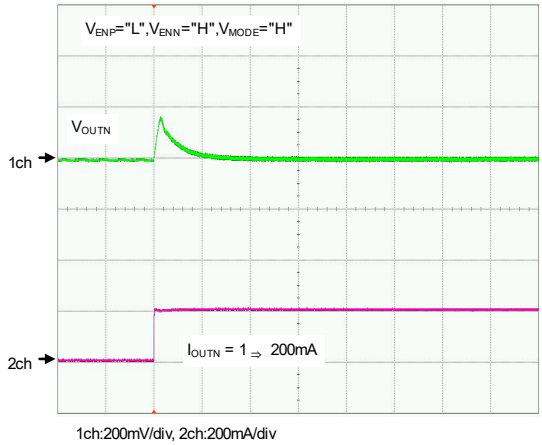
1ch:200mV/div, 2ch:200mA/div

time:500μs/div

Inverting DC/DC Converter: PWM/PFM MODE
(V_{IN}=3.6V, V_{OUTN}=-5.0V, I_{OUTN}=1⇒200mA)

C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

SBD_N: CMS03, R_{ZN}=130kΩ, C_{ZN}=0.47nF



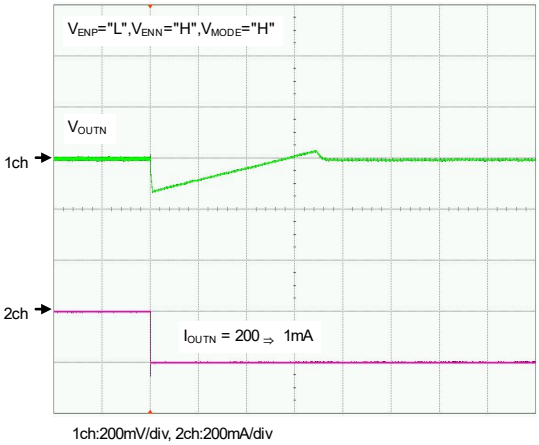
1ch:200mV/div, 2ch:200mA/div

time:100μs/div

Inverting DC/DC Converter: PWM/PFM MODE
(V_{IN}=3.6V, V_{OUTN}=-5.0V, I_{OUTN}=200⇒1mA)

C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

SBD_N: CMS03, R_{ZN}=130kΩ, C_{ZN}=0.47nF



1ch:200mV/div, 2ch:200mA/div

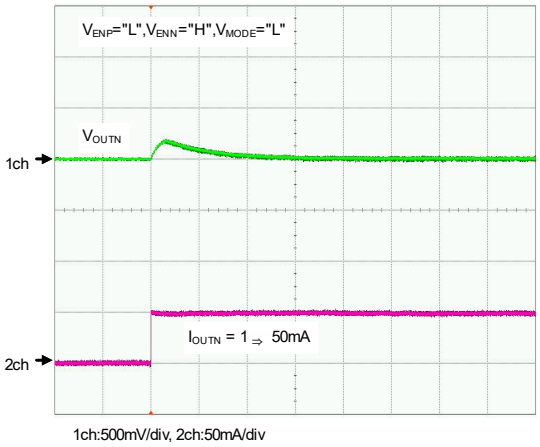
time:500μs/div

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Inverting DC/DC Converter: PWM MODE
(V_{IN}=3.6V, V_{OUTN}=-15.0V, I_{OUTN}=1⇒50mA)

C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

SBD_N: CMS03, R_{ZN}=200kΩ, C_{ZN}=0.47nF



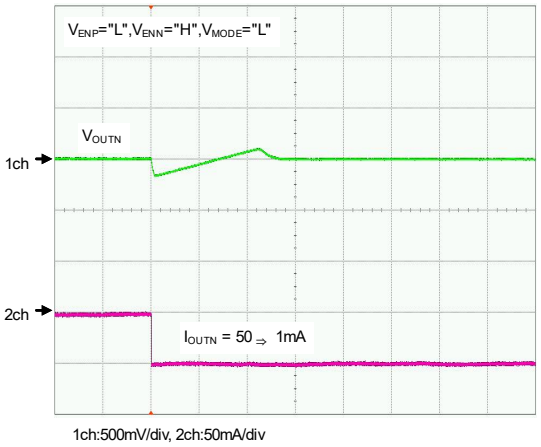
1ch:500mV/div, 2ch:50mA/div

time:100μs/div

Inverting DC/DC Converter: PWM MODE
(V_{IN}=3.6V, V_{OUTN}=-15.0V, I_{OUTN}=50⇒1mA)

C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

SBD_N: CMS03, R_{ZN}=200kΩ, C_{ZN}=0.47nF



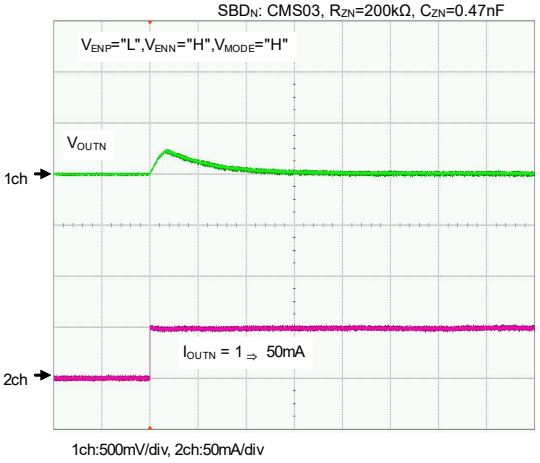
1ch:500mV/div, 2ch:50mA/div

time:500μs/div

Inverting DC/DC Converter: PWM/PFM MODE
(V_{IN}=3.6V, V_{OUTN}=-15.0V, I_{OUTN}=1⇒50mA)

C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

SBD_N: CMS03, R_{ZN}=200kΩ, C_{ZN}=0.47nF



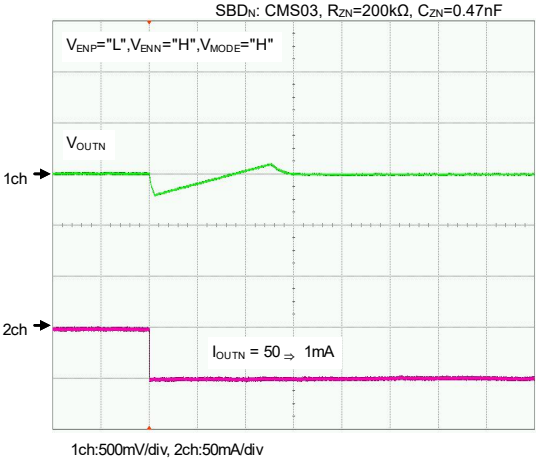
1ch:500mV/div, 2ch:50mA/div

time:100μs/div

Inverting DC/DC Converter: PWM/PFM MODE
(V_{IN}=3.6V, V_{OUTN}=-15.0V, I_{OUTN}=50⇒1mA)

C_{LN}=4×4.7μF, L_N=3.3μH (VLF5014S-3R3M2R0)

SBD_N: CMS03, R_{ZN}=200kΩ, C_{ZN}=0.47nF

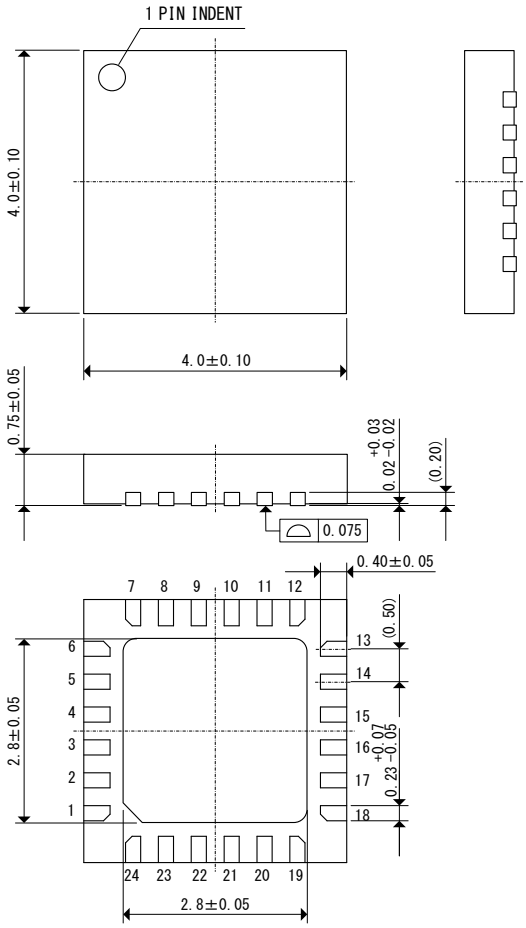


1ch:500mV/div, 2ch:50mA/div

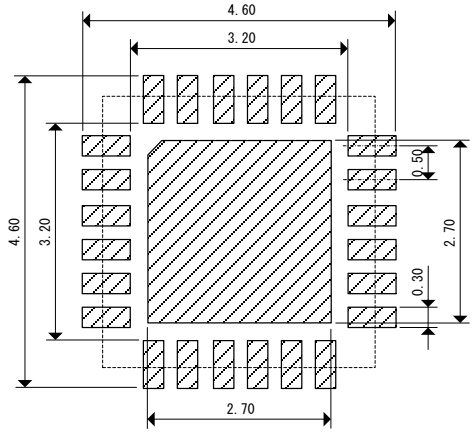
time:500μs/div

■PACKAGING INFORMATION

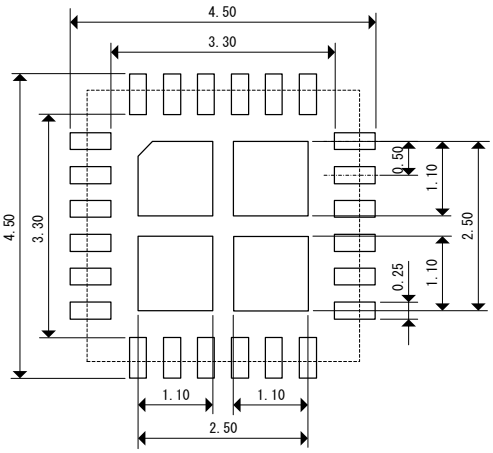
●QFN-24 (unit:mm)



●QFN-24 Reference Pattern Layout (unit:mm)



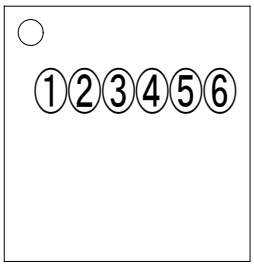
●QFN-24 Reference Metal Mask Design (unit:mm)



■MARKING RULE

QFN-24

1pin



① represent product series.

MARK	PRODUCT SERIES
9	XC9519******-G

② represents UVLO detect voltage.

MARK	UVLO VOLTAGE	PRODUCT SERIES
A	Detect: 2.2V, Hysteresis Width: 0.2V	XC9519A*****-G

③④ represents oscillation frequency and maximum current limit.

MARK		OSCILLATION FREQUENCY	MAXIMUM CURRENT LIMIT	PRODUCT SERIES
③	④			
1	2	1.2MHz	2.0A	XC9519*12A**-G

⑤⑥ represents production lot number.
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, and B1～ZZ repeated
(G, I, J, O, Q, W excluded)
*No character inversion used.

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