

Multi-function voltage detectors with separate sense pin (Max:76V) and low consumption current(0.5μA)

## ■ GENERAL DESCRIPTION

The XC6138 series are high accuracy voltage detectors that can be detected high voltage with sense pin separation and external delay capacitor adjustable type.

The maximum input voltage of the sense pin is 76V, and the detect voltage can be set between 2.3V to 20.0V. This series are capable to monitor high voltage directly and the release voltage can be set between 2.5V to 24.0V as well. Therefore, various combinations of detector voltage and release voltage can be selected.

Since there is no need to divide the voltage by resistance as before, it contributes to higher accuracy of detect/release voltage and lower consumption current of the divider resistor.

The delay time also can be adjusted externally with an external capacitor, and the ratio of detect/release time can be selected. The detect/release time can be set according to the application.

The sense pin is separated from the power input pin, which can maintain the output in the detection state even if the monitoring voltage drops to 0V.

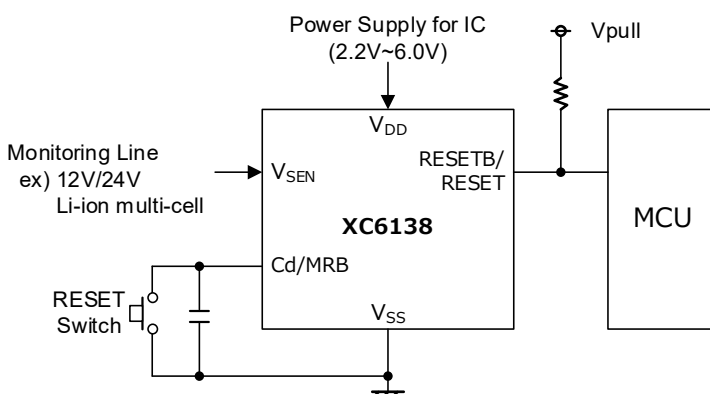
## ■ APPLICATIONS

- Battery voltage monitoring
- System power-on reset
- Microcontroller reset and malfunction monitoring
- Power failure detection

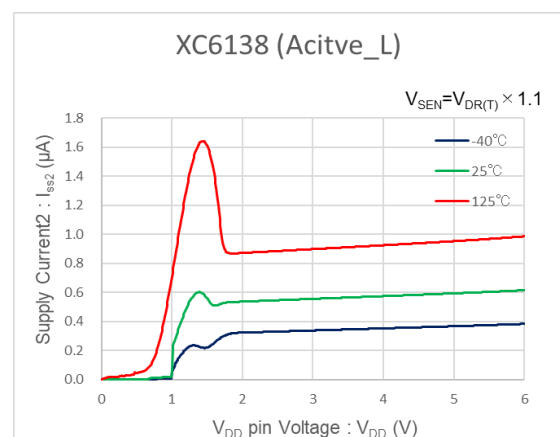
## ■ FEATURES

Operating voltage range	: 2.2V ~ 6.0V
V <sub>SEN</sub> voltage range	: 0.0V ~ 76.0V
Detect voltage range	: 2.3V ~ 20.0V
Release voltage range	: 2.5V ~ 24.0V (+5% ~ +50% of the detect Voltage)
Detect voltage accuracy	: ±1.5%(Ta=25°C), ±3.0%(Ta=-40°C~125°C)
Release voltage accuracy	: ±1.5%(Ta=25°C), ±3.0%(Ta=-40°C~125°C)
Temperature Characteristics	: ±50ppm/°C
Low supply current	: I <sub>DD</sub> 0.5μA @ V <sub>DD</sub> =2.2V I <sub>SEN</sub> 0.15μA @ V <sub>SEN</sub> =12V
Output type	: CMOS output or Nch open drain
Output logic	: H level or L level at detect
Function	: Adjustable detect/release delay time externally Selectable detect/release delay time ratio Manual Reset
Operating ambient temperature	: -40°C ~ 125°C
Packages	: DFN1515-6A (1.5 x 1.5 x 0.38mm) SOT-25 (2.8 x 2.9 x 1.3mm)
Environment friendly	: EU RoHS compliant, Pd free

## ■ TYPICAL APPLICATION CIRCUIT

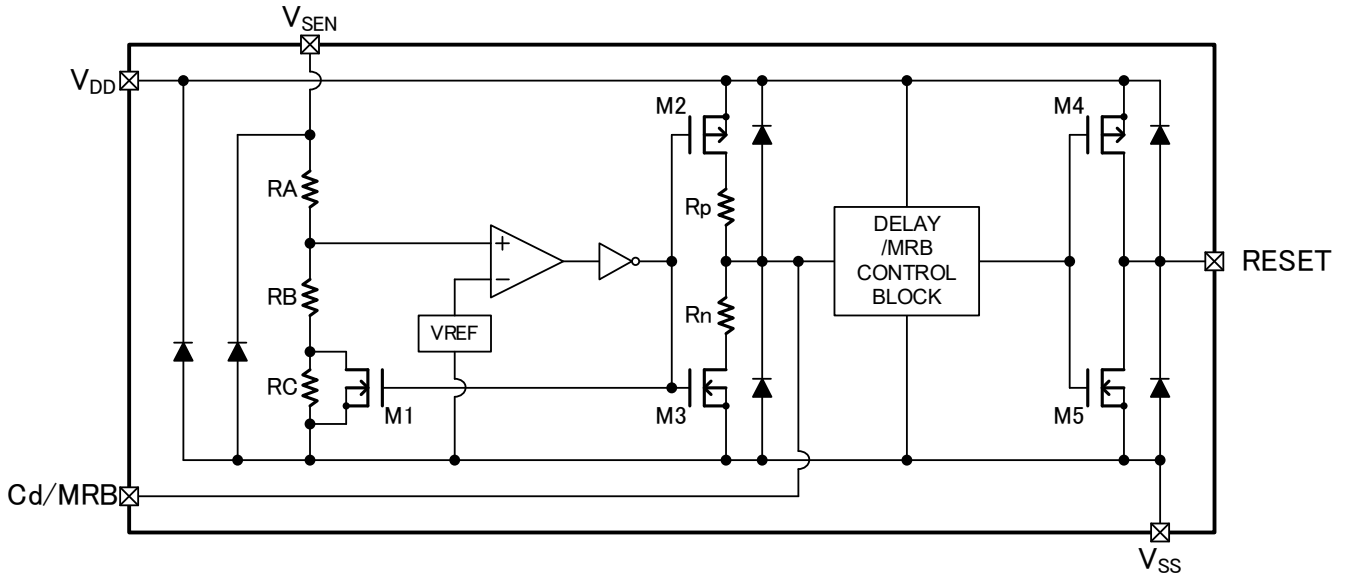


## ■ TYPICAL PERFORMANCE CHARACTERISTICS



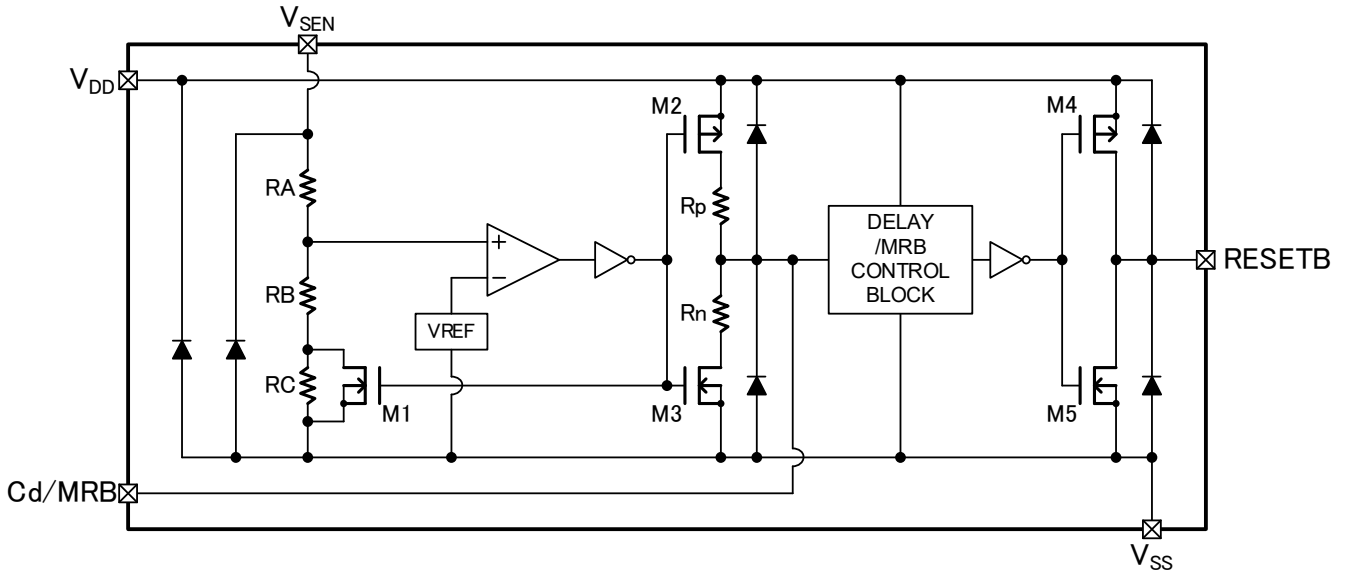
## ■ BLOCK DIAGRAMS

(1) B type : Active "H" / CMOS Output



\* Diodes inside the circuit are ESD protection diode and parasitic diode.

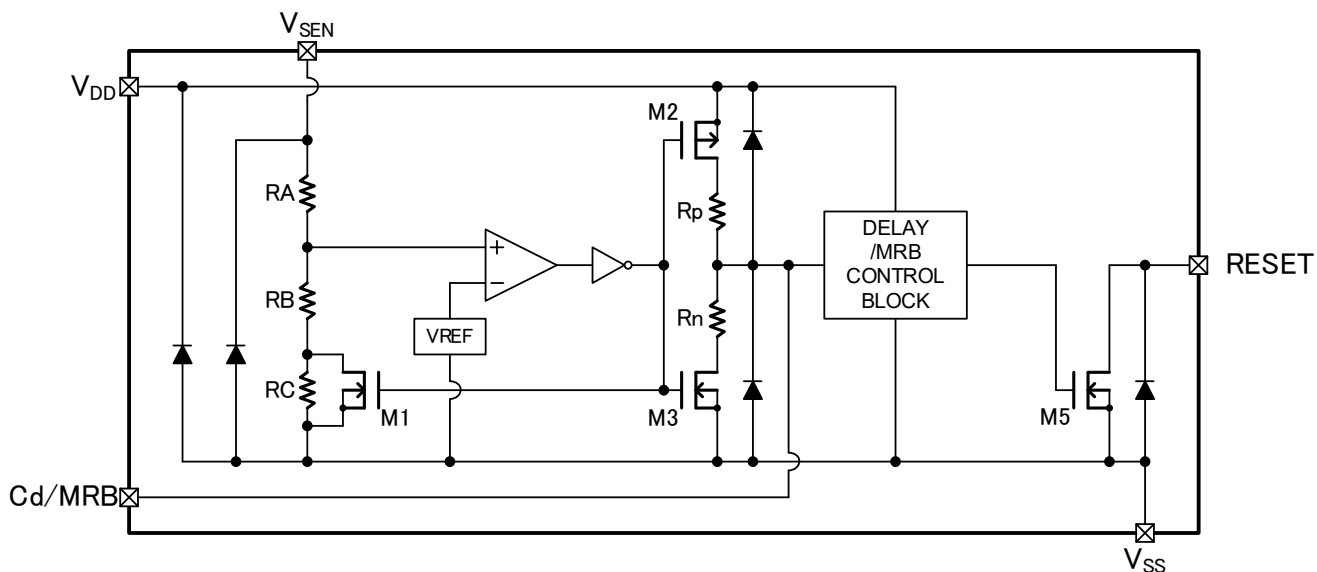
(2) C type : Active "L" / CMOS Output



\* Diodes inside the circuit are ESD protection diode and parasitic diode.

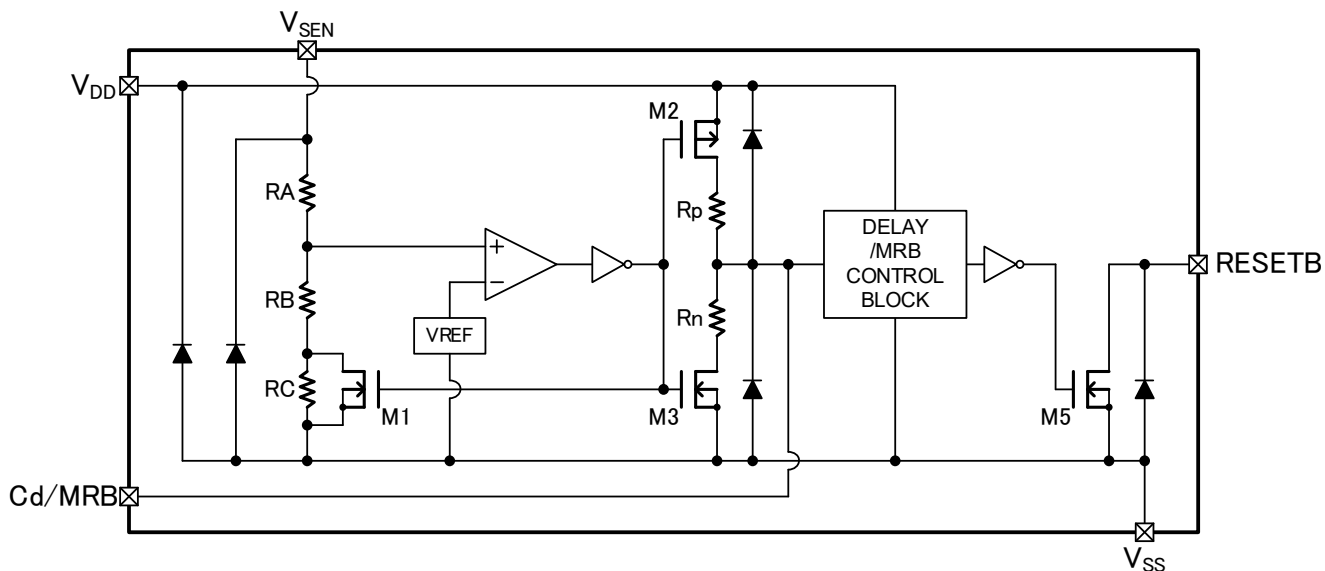
## ■ BLOCK DIAGRAMS (Continued)

(3) M type: Active "H" / Nch Open Drain



\* Diodes inside the circuit are ESD protection diodes and parasitic diodes.

(4) N type: Active "L" / Nch Open Drain



\* Diodes inside the circuit are ESD protection diodes and parasitic diodes.

## PRODUCT CLASSIFICATION

### ●Ordering Information

XC6138①②③④⑤⑥-⑦

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	B	Refer to Selection Guide ①
		C	
		M	
		N	
②	Delay Type /Manual Reset	A ~ H	Refer to Selection Guide ②
③④	Detect Voltage /Release Voltage	01 ~	Refer to Selection Guide ③④
⑤⑥-⑦ (*1)	Package (Order Unit)	6R-G	DFN1515-6A (5,000pcs/Reel)
		MR-G	SOT-25 (3,000pcs/Reel)

(\*1) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

### ●Selection Guide ① : Type

Type ①	Output Configuration	Output Logic	Output Pin Name	Description
B	CMOS output	Active High	RESET	Output High level in detection state.
C		Active Low	RESETB	Output Low level in detection state.
M	Nch open drain	Active High	RESET	Output High level in detection state.
N		Active Low	RESETB	Output Low level in detection state.

### ●Selection Guide ② : Delay Type / Manual Reset

Delay Type ②	Delay Time Ratio (Release Delay:Detect Delay)	Release Delay time (Cd=0.01μF)	Detect Delay time (Cd=0.01μF)	Rp : Rn	Manual Reset function
A	1 : 0.000	10ms	$t_{DF0}^{(*2)}$	1443kΩ : 0kΩ	Yes
B	1 : 0.100	10ms	1ms	1443kΩ : 144.3kΩ	
C	1 : 0.125	10ms	1.25ms	1443kΩ : 180.4kΩ	
D	1 : 0.250	10ms	2.5ms	1443kΩ : 360.8kΩ	
E	1 : 0.500	10ms	5ms	1443kΩ : 721.5kΩ	
F	1 : 1.000	10ms	10ms	1443kΩ : 1443kΩ	
H	0 : 1.000	$t_{DR0}^{(*2)}$	10ms	0kΩ : 1443kΩ	Not available

(\*2)  $t_{DF0}$  : Detect delay time when delay capacitance Cd is not connected.

$t_{DR0}$  : Release delay time when delay capacitance Cd is not connected.

### ●Selection Guide ③④ : Product Code

The detect voltage and release voltage can be specified within the range shown in the below table.

Detect Voltage	Release Voltage	Hysteresis
2.3V ~ 10.0V (0.1V Increments) 10.5V ~ 20.0V (0.5V Increments)	2.5V ~ 10.0V (0.1V Increments) 10.5V ~ 20.0V (0.5V Increments) 21.0V ~ 24.0V (1.0V Increments)	5% ~ 50%(*3)

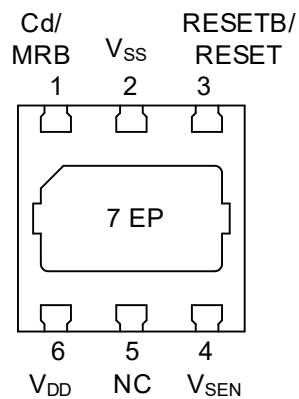
(\*3) Set the detect/release voltage within the setting range of the hysteresis width.

● Standard part number

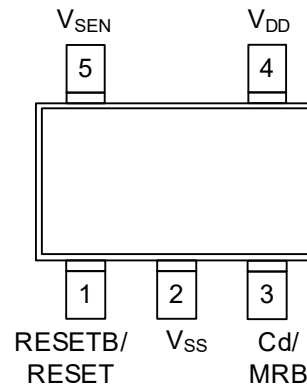
Supposed monitored line	Product Number	Output Configuration	Output Logic	Delay Time Ratio (Release Delay:Detect Delay)	Detect Voltage	Release Voltage	Hysteresis
USB / 5V	XC6138BH7D	CMOS output	Active High	0 : 1.000	5.5V	5.8V	5.5%
	XC6138NA37	Nch open drain	Active Low	1 : 0.000	4.0V	4.2V	5.0%
Li-ion 2cell	XC6138NA94	Nch open drain	Active Low	1 : 0.000	6.0V	6.3V	5.0%
Li-ion 3cell	XC6138NAM1				9.0V	9.5V	5.6%
Li-ion 4cell	XC6138NAP0				12.0V	13.0V	8.3%
Li-ion 5cell	XC6138NAPP				15.0V	16.0V	6.7%
12V	XC6138NANL	Nch open drain	Active Low	1 : 0.000	10.0V	10.5V	5.0%
	XC6138NAN0				9.5V	10.0V	5.3%
	XC6138NARJ				7.5V	9.7V	29.3%
	XC6138NCN0			1 : 0.125	9.5V	10.0V	5.3%
	XC6138NCRJ				7.5V	9.7V	29.3%
	XC6138NAL6	1 : 0.000	8.7V	9.2V	5.7%		
	XC6138CAN0	CMOS output	Active Low	1 : 0.000	9.5V	10.0V	5.3%
	XC6138CCN0			1 : 0.125			
	XC6138CARJ			1 : 0.000	7.5V	9.7V	29.3%
XC6138CCRJ	1 : 0.125						
15V	XC6138NAP0	Nch open drain	Active Low	1 : 0.000	12.0V	13.0V	8.3%
	XC6138NARZ				10.0V	13.0V	30.0%
20V	XC6138NAPZ	Nch open drain	Active Low	1 : 0.000	16.0V	17.0V	6.3%
	XC6138NAPN				14.5V	17.0V	17.2%
24V	XC6138NAQZ	Nch open drain	Active Low	1 : 0.000	20.0V	21.0V	5.0%
	XC6138NAQT				19.0V	20.0V	5.3%
	XC6138NASY				15.5V	20.0V	29.0%
	XC6138NAQE				17.5V	18.5V	5.7%

With regard to other voltage, please contact our sales representative.

## PIN CONFIGURATION



DFN1515-6A  
(BOTTOM VIEW)



SOT-25  
(TOP VIEW)

## PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTIONS
DFN1515-6A	SOT-25		
1	3	Cd/MRB	Adjustable Pin for Delay Time / Manual Reset (Delay Type : A ~ F)
			Adjustable Pin for Delay Time (Delay Type : H)
2	2	V <sub>SS</sub>	Ground
3	1	RESETB	Reset Output (Active "L")
		RESET	Reset Output (Active "H")
4	5	V <sub>SEN</sub>	Voltage Sense
5	-	NC	No Connection
6	4	V <sub>DD</sub>	Power Supply Input
7	-	EP	Exposed thermal pad. The Exposed pad is recommended to be connected to V <sub>SS</sub> (Pin2)

## FUNCTION CHART

Type	Output Configuration	Output Logic	Reset Output		
			Release State	Detection State or Manual RESET (V <sub>Cd/MRB</sub> ≤ V <sub>MR</sub> )	Undefined State (V <sub>DD</sub> < 2.2V)
C	CMOS output	Active Low	"H" (V <sub>DD</sub> )	"L" (V <sub>SS</sub> )	Undefined
B		Active High	"L" (V <sub>SS</sub> )	"H" (V <sub>DD</sub> )	Undefined
N	Nch open drain	Active Low	"H" (V <sub>pull</sub> : High impedance)	"L" (V <sub>SS</sub> : Low Impedance)	Undefined
M		Active High	"L" (V <sub>SS</sub> : Low Impedance)	"H" (V <sub>pull</sub> : High impedance)	Undefined

## ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
V <sub>DD</sub> Pin Voltage		V <sub>DD</sub>	-0.3 ~ 6.5	V
V <sub>SEN</sub> Pin Voltage		V <sub>SEN</sub>	-0.3 ~ 80.0	V
V <sub>SEN</sub> Pin Surge Voltage		V <sub>SURGE</sub>	90 <sup>(*)3</sup>	V
Cd/MRB Pin Voltage		V <sub>Cd/MRB</sub>	V <sub>SS</sub> - 0.3 ~ V <sub>DD</sub> + 0.3 or 6.5 <sup>(*)1</sup>	V
Cd/MRB Pin Current <sup>(*)4</sup>		I <sub>Cd/MRB</sub>	-20 ~ 20	mA
Output Current	CMOS	I <sub>RBOUT</sub> / I <sub>ROUT</sub>	-50 ~ 50	mA
	Nch open drain		50	mA
Power Dissipation (Ta=25°C)	DFN1515-6A	Pd	1000 (40mm x 40mm standard board) <sup>(*)2</sup>	mW
	SOT-25		950 (JESD51-7 board) <sup>(*)2</sup>	
Junction Temperature		T <sub>j</sub>	-40 ~ 150	°C
Storage Temperature		T <sub>stg</sub>	-55 ~ 150	°C

\* All voltages are described based on the V<sub>SS</sub>.

(\*)1 The maximum value should be either V<sub>DD</sub>+0.3V or 6.5V in the lowest.

(\*)2 This is a reference data taken by using the test board.

Please refer to PACKAGING INFORMATION for the mounting condition.

(\*)3 Transient ≤ 400ms

(\*)4 When the following voltages are applied to the Cd/MRB pin, current flows outside the recommended operating range.

Take countermeasures by connecting a limiting resistor or similar so that the Cd/MRB pin current is within the recommended operating range.

- Delay type A : Cd/MRB "H" level voltage @ detect status
- Delay type H : Cd/MRB "L" level voltage @ release status

## ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNITS
V <sub>DD</sub> Pin Voltage		V <sub>DD</sub>	2.2	-	6.0	V
V <sub>SEN</sub> Input Voltage		V <sub>SEN</sub>	0.0	-	76.0	V
Cd/MRB Pin Voltage		V <sub>Cd/MRB</sub>	0.0		V <sub>DD</sub>	V
Nch open drain	Pull-up Voltage	V <sub>pull</sub>	0.0	-	6.0	V
	Pull-up Resistance	I <sub>ROUT</sub>	1	100	-	kΩ
Operating Ambient Temperature		T <sub>opr</sub>	-40	-	125	°C
Junction Temperature		T <sub>j</sub>	-40	-	125	°C
Cd Capacitor		Cd	OPEN	-	10000	nF

\* All voltages are described based on the V<sub>SS</sub>.

## ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Ta=25°C			-40°C ≤ Ta ≤ 125°C <sup>(6)</sup>			UNITS	CIRCUIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Operating Voltage	V <sub>DD</sub>		2.2	-	6.0	2.2	-	6.0	V	①
V <sub>SEN</sub> Input Voltage	V <sub>SEN</sub>		0.0	-	76.0	0.0	-	76.0	V	
Detect Voltage	V <sub>DF</sub>	V <sub>DF</sub> =2.3V ~ 20.0V	V <sub>DF(T)</sub> ×0.985	V <sub>DF(T)</sub>	V <sub>DF(T)</sub> ×1.015	V <sub>DF(T)</sub> ×0.97	V <sub>DF(T)</sub>	V <sub>DF(T)</sub> ×1.03	V	
Release Voltage	V <sub>DR</sub>	V <sub>DR</sub> =2.5V ~ 24.0V	V <sub>DR(T)</sub> ×0.985	V <sub>DR(T)</sub>	V <sub>DR(T)</sub> ×1.015	V <sub>DR(T)</sub> ×0.97	V <sub>DR(T)</sub>	V <sub>DR(T)</sub> ×1.03	V	
Hysteresis Width	HYS	HYS=(V <sub>DR</sub> -V <sub>DF</sub> )/V <sub>DF</sub> ×100	HYS <sub>(T)</sub> -2.3	HYS <sub>(T)</sub>	HYS <sub>(T)</sub> +2.3	HYS <sub>(T)</sub> -2.4	HYS <sub>(T)</sub>	HYS <sub>(T)</sub> +2.4	%	
Temperature Characteristics	$\frac{\Delta V_{DF}}{(\Delta T_{opr} \cdot V_{DF})}$	-40°C ≤ Topr ≤ 125°C	-	±50	-	-	±50	-	ppm/°C	
Supply Current 1	I <sub>DD1</sub>	V <sub>SEN</sub> =V <sub>DF</sub> ×0.9, V <sub>DD</sub> =2.2V	-	0.48	1.27	-	0.48	1.78	μA	②
		V <sub>SEN</sub> =V <sub>DF</sub> ×0.9, V <sub>DD</sub> =6.0V	-	0.50	1.30	-	0.50	1.8		
Supply Current 2	I <sub>DD2</sub>	V <sub>SEN</sub> =V <sub>DR</sub> ×1.1, V <sub>DD</sub> =2.2V	-	0.54	1.40	-	0.54	2.00	μA	②
		V <sub>SEN</sub> =V <sub>DR</sub> ×1.1, V <sub>DD</sub> =6.0V	-	0.60	1.59	-	0.60	2.24		
SENSE Resistance	R <sub>SEN</sub>	V <sub>DD</sub> =6.0V, V <sub>SEN</sub> =2.2V	12	80	-	7.3	80	-	MΩ	③
Detect Delay Resistance	R <sub>n</sub>	Delay Type : B V <sub>DD</sub> =6.0V, V <sub>SEN</sub> =0V V <sub>Cd/MRB</sub> =6.0V	130	144.3	158	129	144.3	210	kΩ	④
		Delay Type : C V <sub>DD</sub> =6.0V, V <sub>SEN</sub> =0V V <sub>Cd/MRB</sub> =6.0V	166	180.4	194	164	180.4	235		
		Delay Type : D V <sub>DD</sub> =6.0V, V <sub>SEN</sub> =0V V <sub>Cd/MRB</sub> =6.0V	334	360.8	386	330	360.8	432		
		Delay Type : E V <sub>DD</sub> =6.0V, V <sub>SEN</sub> =0V V <sub>Cd/MRB</sub> =6.0V	681	721.5	759	627	721.5	883		
		Delay Type : F, H V <sub>DD</sub> =6.0V, V <sub>SEN</sub> =0V V <sub>Cd/MRB</sub> =6.0V	1361	1443	1522	1307	1443	1545		
Release Delay Resistance	R <sub>p</sub>	Delay Type : A,B,C,D,E,F V <sub>DD</sub> =6.0V, V <sub>SEN</sub> =60.0V V <sub>Cd/MRB</sub> =0V	1361	1443	1522	1307	1443	1545		
Release Delay Time <sup>(4)</sup>	t <sub>DR0</sub>	V <sub>DD</sub> =6.0V, V <sub>SEN</sub> =V <sub>DF</sub> ×0.9→V <sub>DR</sub> ×1.1	-	156.5	-	-	156.5	497	μs	⑤
Detect Delay Time <sup>(5)</sup>	t <sub>DF0</sub>	V <sub>DD</sub> =6.0V, V <sub>SEN</sub> =V <sub>DR</sub> ×1.1→V <sub>DF</sub> ×0.9	-	74.4	-	-	74.4	230		

Unless otherwise specified in measurement conditions, Cd/MRB pin are open.

<sup>(1)</sup> V<sub>DF(T)</sub> : Nominal detect voltage

<sup>(2)</sup> V<sub>DR(T)</sub> : Nominal release voltage

<sup>(3)</sup> HYS<sub>(T)</sub> : Nominal hysteresis width (V<sub>DR(T)</sub>-V<sub>DF(T)</sub>)/V<sub>DF(T)</sub>×100

<sup>(4)</sup> RESETB product : Time from when the V<sub>SEN</sub> pin voltage reaches the release voltage until the reset output pin reaches V<sub>DD</sub>×90%.

RESET product : V<sub>SEN</sub> Time from when the V<sub>SEN</sub> pin voltage reaches the release voltage until the reset output pin reaches V<sub>DD</sub>×10%.

<sup>(5)</sup> RESETB product : Time from when the V<sub>SEN</sub> pin voltage reaches the detect voltage until the reset output pin reaches V<sub>DD</sub>×10%.

RESET product : Time from when the V<sub>SEN</sub> pin voltage reaches the detect voltage until the reset output pin reaches V<sub>DD</sub>×90%.

<sup>(6)</sup> The ambient temperature range (-40°C ≤ Ta ≤ 125°C) is a design Value.



**■ ELECTRICAL CHARACTERISTICS (Continued)**

PARAMETER	SYMBOL	CONDITIONS	Ta=25°C			-40°C ≤ Ta ≤ 125°C <sup>(*)6</sup>			UNITS	CIRC UIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
RESETB Output Current	I <sub>RBOUTN</sub>	V <sub>SEN</sub> =V <sub>DF</sub> ×0.9, Nch. V <sub>RESETB</sub> =0.05V V <sub>DD</sub> =2.2V	2.07	3.57	-	1.1	3.57	-	mA	⑥
	I <sub>RBOUTP</sub>	V <sub>SEN</sub> =V <sub>DR</sub> ×1.1, Pch. V <sub>RESETB</sub> =V <sub>DD</sub> -0.05V V <sub>DD</sub> =2.2V	-	-0.49	-0.36	-	-0.49	-0.3		
RESET Output Current	I <sub>ROUTN</sub>	V <sub>SEN</sub> =V <sub>DR</sub> ×1.1, Nch. V <sub>RESETB</sub> =0.05V V <sub>DD</sub> =2.2V	2.07	3.57	-	1.1	3.57	-	mA	
	I <sub>ROUTP</sub>	V <sub>SEN</sub> =V <sub>DF</sub> ×0.9, Pch. V <sub>RESETB</sub> =V <sub>DD</sub> -0.05V V <sub>DD</sub> =2.2V	-	-0.49	-0.36	-	-0.49	-0.3		
RESETB Output Leakage Current	I <sub>LEAKN</sub> <sup>(*)7</sup>	V <sub>DD</sub> =6.0V, V <sub>SEN</sub> =60.0V Nch. V <sub>RESETB</sub> =6.0V	-	0.01	0.1	-	0.01	0.3	μA	
	I <sub>LEAKP</sub>	V <sub>DD</sub> =6.0V, V <sub>SEN</sub> =0V Pch. V <sub>RESETB</sub> =0V	-	-0.01	-	-	-0.01	-		
RESET Output Leakage Current	I <sub>LEAKN</sub> <sup>(*)7</sup>	V <sub>DD</sub> =6.0V, V <sub>SEN</sub> =0V Nch. V <sub>RESET</sub> =6.0V	-	0.01	0.1	-	0.01	0.3	μA	
	I <sub>LEAKP</sub>	V <sub>DD</sub> =6.0V, V <sub>SEN</sub> =60.0V Pch. V <sub>RESET</sub> =0V	-	-0.01	-	-	-0.01	-		
Cd/MRB Pin Source Current (Delay Type : A)	I <sub>CdSource</sub>	V <sub>DD</sub> =2.2V, V <sub>SEN</sub> =0V Nch. V <sub>Cd/MRB</sub> =0.3V	0.97	1.40	-	0.89	1.40	-	mA	④
Cd/MRB Pin Sink Current (Delay Type : H)	I <sub>CdSink</sub>	V <sub>DD</sub> =2.2V, V <sub>SEN</sub> =60V Pch. V <sub>Cd/MRB</sub> =V <sub>DD</sub> -0.3V	-	-1.00	-0.78	-	-1.00	-0.76		
Cd Threshold Voltage (Release)	V <sub>TCd1</sub>	V <sub>DD</sub> :2.2V ~ 6.0V, V <sub>SEN</sub> =0V→V <sub>DR</sub> ×1.1	V <sub>DD</sub> × 0.475	V <sub>DD</sub> × 0.50	V <sub>DD</sub> × 0.525	V <sub>DD</sub> × 0.475	V <sub>DD</sub> × 0.50	V <sub>DD</sub> × 0.525	V	⑦
Cd Threshold Voltage (Detect)	V <sub>TCd2</sub>	V <sub>DD</sub> :2.2V ~ 6.0V, V <sub>SEN</sub> =V <sub>DR</sub> ×1.1→0V								
MRB Threshold Voltage	V <sub>MR</sub> <sup>(*)8</sup>	V <sub>DD</sub> :2.2V ~ 6.0V, V <sub>SEN</sub> =V <sub>DR</sub> ×1.1	V <sub>DD</sub> × 0.475	V <sub>DD</sub> × 0.50	V <sub>DD</sub> × 0.525	V <sub>DD</sub> × 0.475	V <sub>DD</sub> × 0.50	V <sub>DD</sub> × 0.525	V	
MRB Minimum Pulse Width (B,C,N Type)	t <sub>MRIN</sub> <sup>(*)8</sup>	V <sub>DD</sub> :2.2V ~ 6.0V V <sub>SEN</sub> =V <sub>DR</sub> ×1.1, Apply pulse from V <sub>DD</sub> to 0V to the Cd/MRB pin.	9	-	-	10	-	-	μs	⑧
MRB Minimum Pulse Width (M Type)			30	-	-	30	-	-		

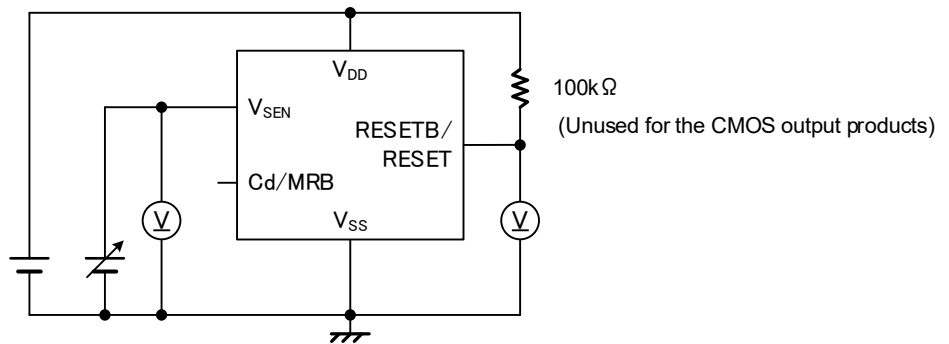
Unless otherwise specified in measurement conditions, Cd/MRB pin are open.

<sup>(\*)7</sup> Max. value is for XC6138M/N (Nch open drain).

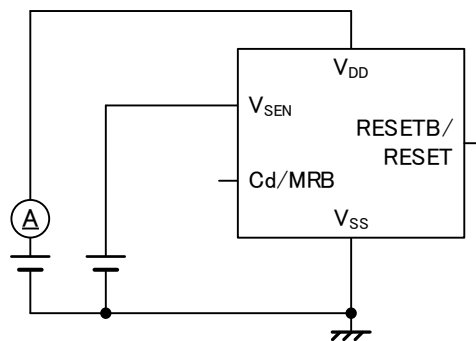
<sup>(\*)8</sup> Delay Type H (Rp:Rn=0kΩ : 1443kΩ) does not have a Manual reset function.

## TEST CIRCUITS

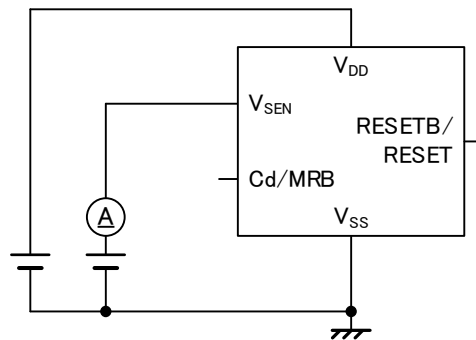
CIRCUIT①



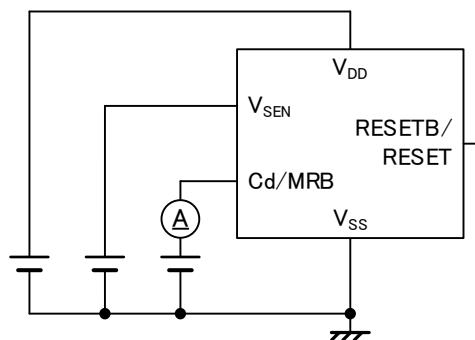
CIRCUIT②



CIRCUIT③

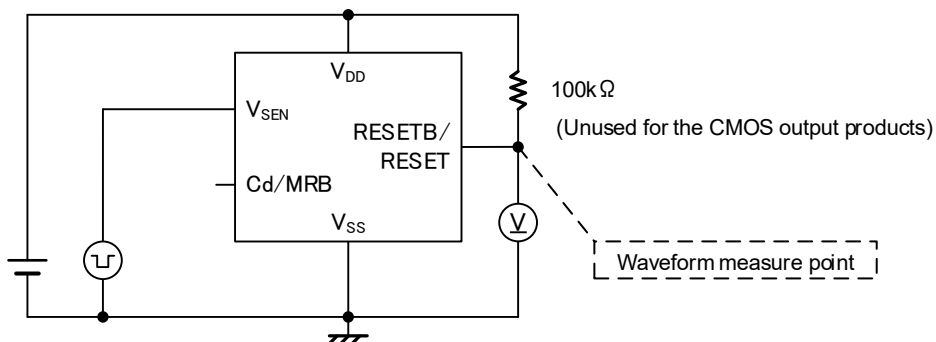


CIRCUIT④

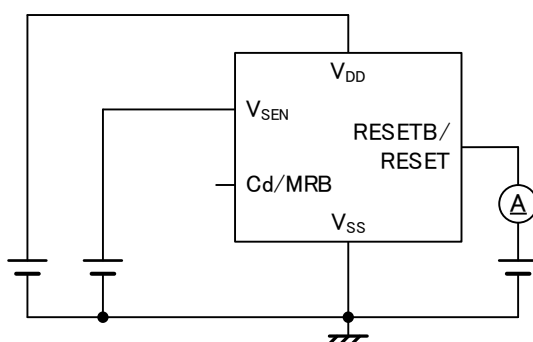


■ TEST CIRCUITS (Continued)

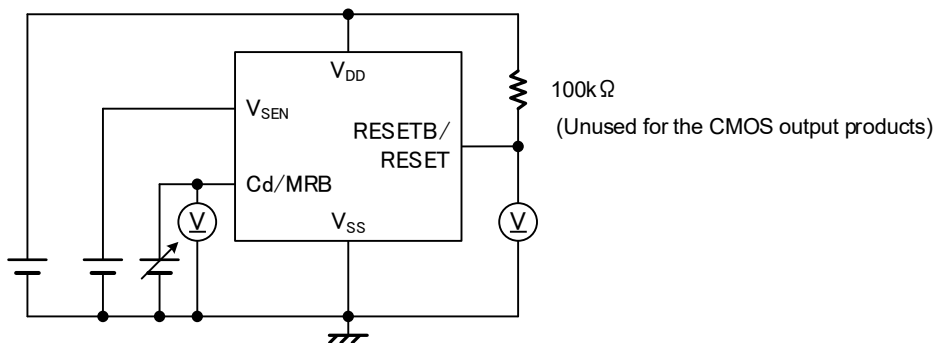
CIRCUIT⑤



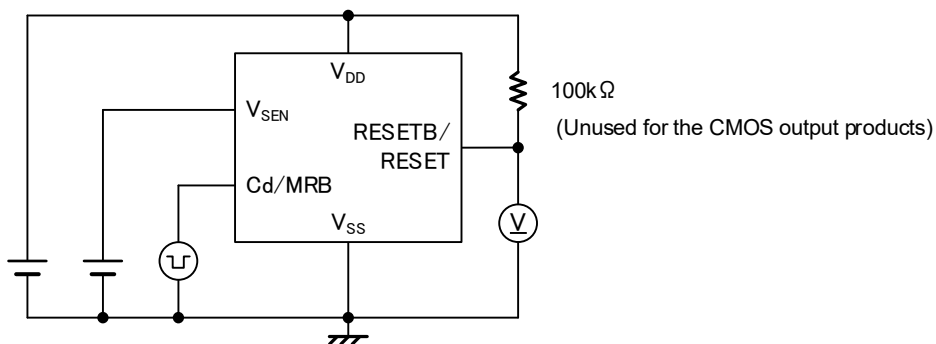
CIRCUIT⑥



CIRCUIT⑦



CIRCUIT⑧



## OPERATIONAL DESCRIPTION

<General operation : Active Low (Type: C,N)>

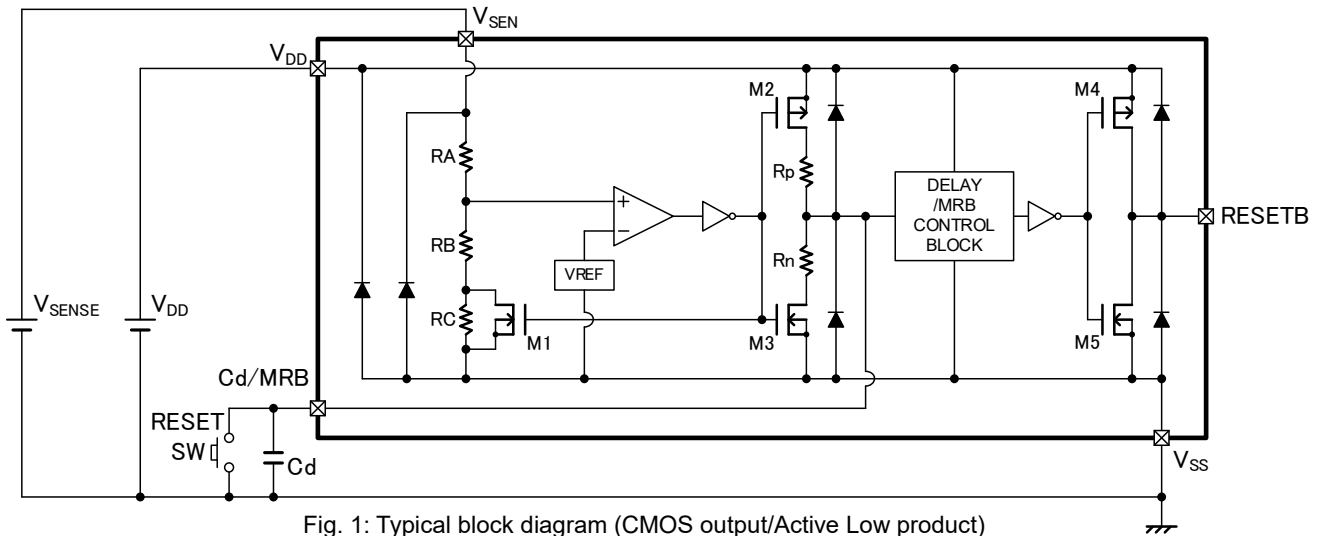


Fig. 1: Typical block diagram (CMOS output/Active Low product)

The circuit operation of the Active Low product will be explained using the timing chart.

① Release state

When the  $V_{SEN}$  pin voltage is higher than  $V_{DF}$ , the device is released and the RESETB pin voltage becomes a "H" output. In this state, the delay capacitance  $C_d$  will rise in voltage up to  $V_{DD}$ .

② Release state → Detect state

When the  $V_{SEN}$  pin voltage drops below the detect voltage ( $V_{DF}$ ), it enters the detect state. In the detect state, Nch FETs M1 and M3 are turned on, and the delay capacitance  $C_d$  is discharged through the detect delay resistor  $R_n$ . When the  $C_d/MRB$  pin voltage drops to  $V_{TCd2}$  (TYP.  $V_{DD} \times 0.50$ ), the RESETB pin voltage outputs a "L" level signal. By turning on the FET between  $C_d/MRB$  and  $V_{SS}$ , the  $C_d/MRB$  pin voltage is discharged rapidly.

③ Detect state → Release state

The  $V_{SEN}$  pin voltage rises and becomes higher than  $V_{DR}$ , it enters the release state. In the release state, the Nch FET M1 and M3 are turned off and M2 is turned on, and the delay capacitor  $C_d$  is charged through the release delay resistor  $R_p$ . When the  $C_d/MRB$  pin voltage rises to  $V_{TCd1}$  (TYP.  $V_{DD} \times 0.50$ ), the RESETB pin voltage outputs a "H" level signal. By turning on the FET between  $C_d/MRB$  and  $V_{DD}$ , the  $C_d/MRB$  pin voltage is charged rapidly.

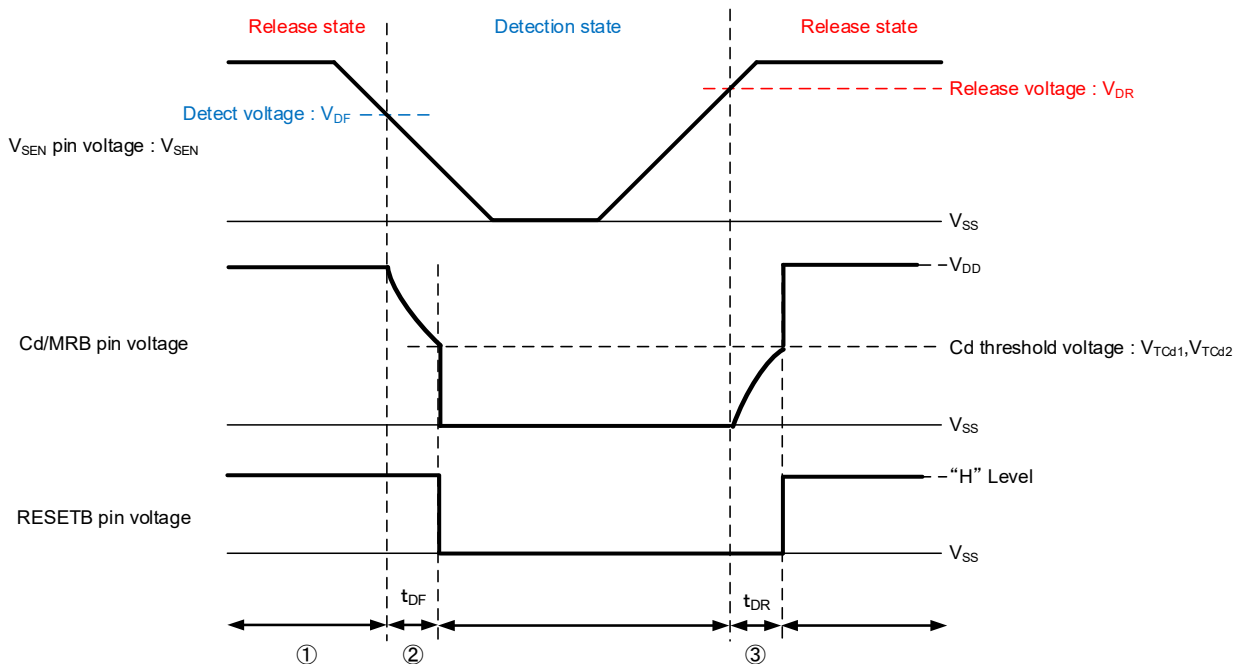


Fig. 2: Timing chart (Active Low product)

## OPERATIONAL DESCRIPTION

<General operation : Active High (Type: B,M)>

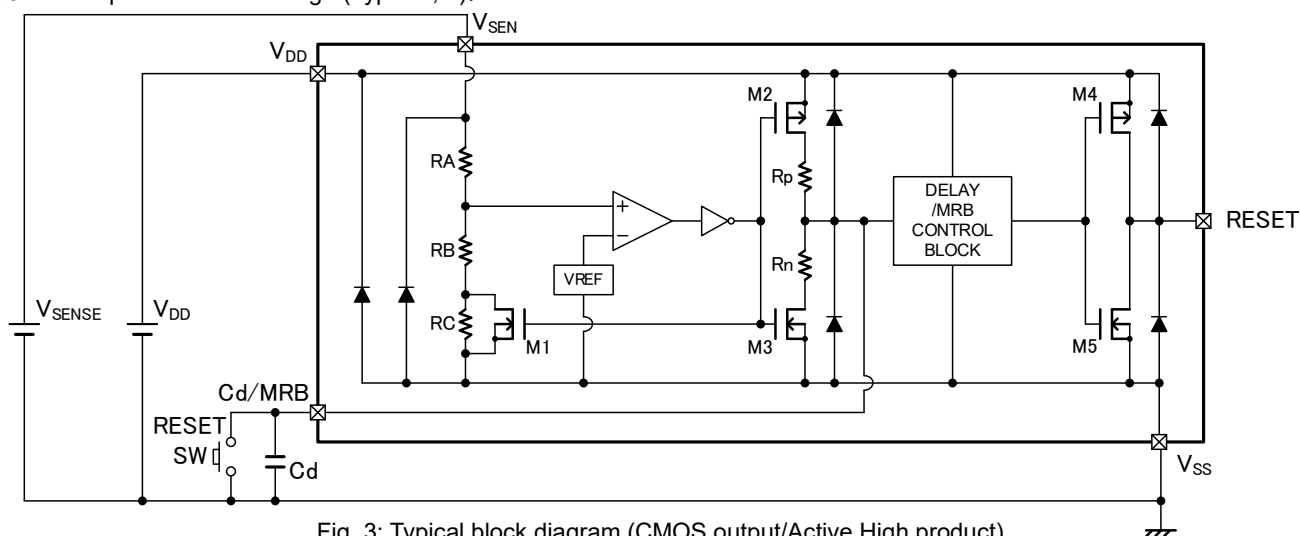


Fig. 3: Typical block diagram (CMOS output/Active High product)

The circuit operation of the Active High product will be explained using the timing chart.

### ① Release state

When the  $V_{SEN}$  pin voltage is higher than  $V_{DF}$ , the device is released and the RESET pin voltage outputs a "L" level signal. In this state, the delay capacitance  $C_d$  will rise in voltage up to  $V_{DD}$ .

### ② Release state → Detect state

When the  $V_{SEN}$  pin voltage drops below the detect voltage ( $V_{DF}$ ), it enters the detect state.

In the detect state, Nch FETs M1 and M3 are turned on, and the delay capacitance  $C_d$  is discharged through the detection delay resistor  $R_n$ .

When the  $C_d/MRB$  pin voltage drops to  $V_{TCd2}$  (TYP.  $V_{DD} \times 0.50$ ), the RESET pin voltage outputs a "H" level signal. By turning on the FET between  $C_d/MRB$  and  $V_{SS}$ , the  $C_d/MRB$  pin voltage is discharged rapidly.

### ③ Detect state → Release state

The  $V_{SEN}$  pin voltage rises and becomes higher than  $V_{DR}$ , it enters the release state.

In the release state, the Nch FET M1 and M3 are turned off and M2 is turned on, and the delay capacitor  $C_d$  is charged through the release delay resistor  $R_p$ .

When the  $C_d/MRB$  pin voltage rises to  $V_{TCd1}$  (TYP.  $V_{DD} \times 0.50$ ), the RESET pin voltage outputs a "L" level signal. By turning on the FET between  $C_d/MRB$  and  $V_{DD}$ , the  $C_d/MRB$  pin voltage is charged rapidly.

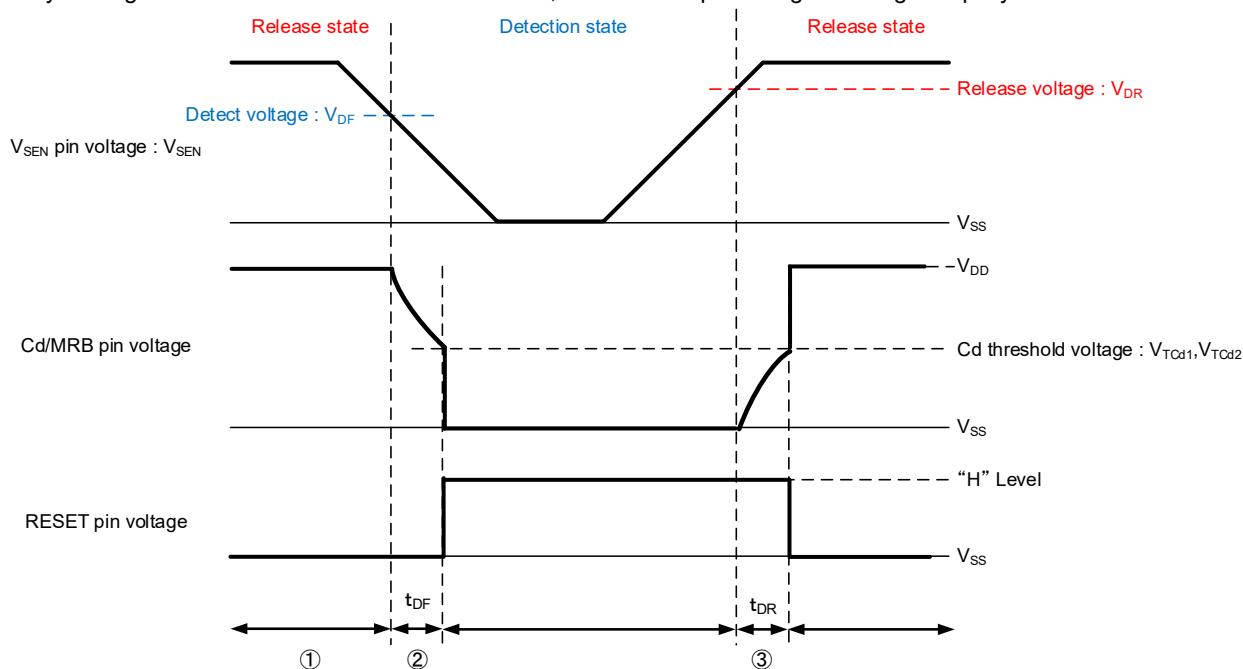


Fig. 4: Timing chart (Active High product)

## OPERATIONAL DESCRIPTION

<Release delay time/Detect delay time>

The release delay time and detect delay time are determined by the delay resistors (Rp and Rn) and the delay capacitance Cd. The ratio of the delay resistances (Rp and Rn) depending on the Delay Type, and can be selected from the following combinations.

Delay Type	Delay Time Ratio (Release Delay:Detect Delay)	Release Delay time (Cd=0.01μF)	Detect Delay time (Cd=0.01μF)	Rp	Rn
A	1 : 0.000	10ms	t <sub>DF0</sub> <sup>(*)</sup>	1443kΩ	0kΩ
B	1 : 0.100	10ms	1ms	1443kΩ	144.3kΩ
C	1 : 0.125	10ms	1.25ms	1443kΩ	180.4kΩ
D	1 : 0.250	10ms	2.5ms	1443kΩ	360.8kΩ
E	1 : 0.500	10ms	5ms	1443kΩ	721.5kΩ
F	1 : 1.000	10ms	10ms	1443kΩ	1443kΩ
H	0 : 1.000	t <sub>DR0</sub> <sup>(*)</sup>	10ms	0kΩ	1443kΩ

<sup>(\*)</sup> t<sub>DF0</sub> : Detect delay time when delay capacitance Cd is not connected.

t<sub>DR0</sub> : Release delay time when delay capacitance Cd is not connected.

The release delay time (t<sub>DR</sub>) and detect delay time are calculated using Equation (1-1) and Equation (2-1).

$$t_{DR} = R_p \times C_d \times \{-\ln(1 - V_{TCD1}/V_{DD})\} + t_{DR0} \quad (1-1)$$

$$t_{DF} = R_n \times C_d \times \{-\ln(V_{TCD2}/V_{DD})\} + t_{DF0} \quad (2-1)$$

\* ln is the natural logarithm.

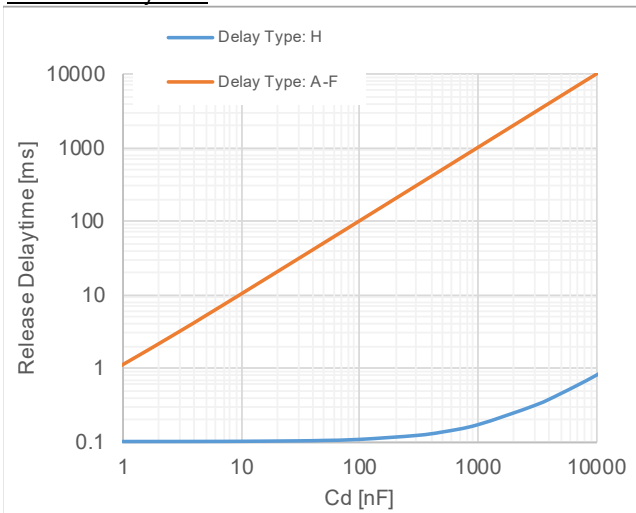
Since the Cd threshold voltages V<sub>TCD1</sub> and V<sub>TCD2</sub> are V<sub>DD</sub> × 0.50 (TYP.), the release delay time can be calculated simply using Equation (1-1) and Equation (2-1).

$$t_{DR} = R_p \times C_d \times 0.693 + t_{DR0} \quad (1-2)$$

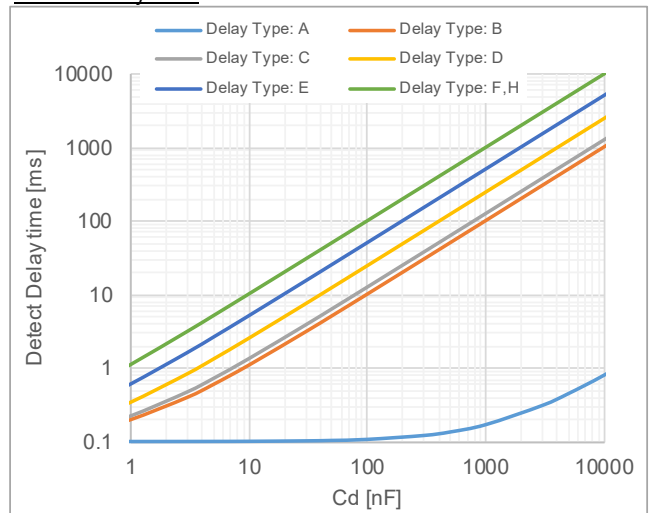
$$t_{DF} = R_n \times C_d \times 0.693 + t_{DF0} \quad (2-2)$$

\* ln is the natural logarithm.

Release Delay time



Detect Delay time



## OPERATIONAL DESCRIPTION

<Manual reset function>

Delay Type : A-F

The manual reset function is a feature that forcibly puts the device in the detect state from the release state. The manual reset function can be used by connecting a physical switch or FET to the Cd/MRB pin.

When the Cd/MRB pin voltage falls below the MRB threshold voltage in the release state, the manual reset function is activated and the device transitions from the release state to the detect state. When the manual reset function puts the device in the detect state, no detect delay time is incurred.

Delay Type : H

Delay Type H may not activate the manual reset function depending on the bias conditions and SW, etc. Therefore, We do not recommended to use the manual reset function for Delay Type H.

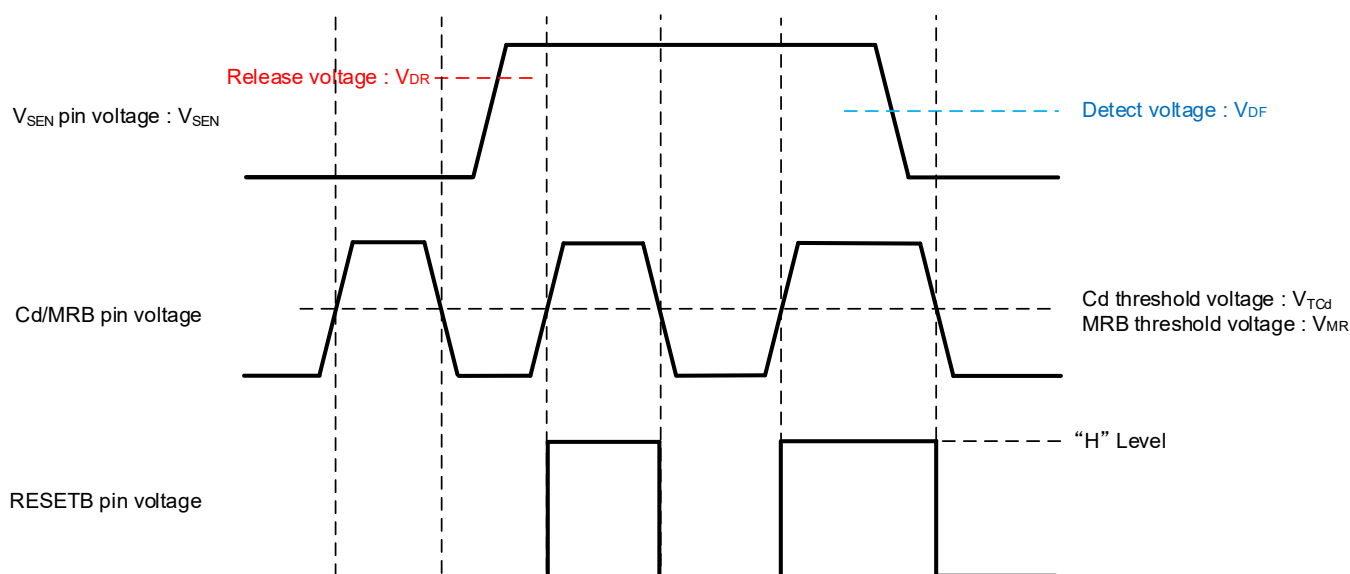


Fig. 5. Manual reset operation (Active Low)

## OPERATIONAL DESCRIPTION

<Select guide for pull-up resistor (Nch open drain: N,M Type)>

When an Nch open drain output is used, a pull-up resistor connected to the RESET/RESETB pin causes a deviation in the output voltage between the  $V_{SS}$  and  $V_{DD}$  voltages.

To reduce the deviation in the output voltage between the  $V_{SS}$  and  $V_{DD}$  voltages, connect a pull-up resistor of around 10k $\Omega$  to several 100k $\Omega$ .

If the resistance value of pull-up resistor is small, the deviation from  $V_{SS}$  becomes large and it is impossible to meet the "L" voltage of the MCU.

Similarly, if the resistance value of pull-up resistor is large, the deviation from  $V_{DD}$  becomes large and it is impossible to meet the "H" voltage.

In the actual specifications, select a pull-up resistor that meets the logic threshold of the subsequent IC.

Below is an example calculation of the maximum output "L" voltage and the minimum output "H" voltage.

### 【Maximum value of output "L" voltage】

$$V_{\text{RESETB}} = V_{\text{pull}} / (1 + R_{\text{pull}} / R_{\text{ON\_MAX}})$$

$V_{\text{pull}}$  : Pull-up voltage

$R_{\text{ON\_MAX}}$  : On resistor maximum value of Nch driver M5.

Calculation Example)  $V_{\text{DD}}=2.2\text{V}$ ,  $V_{\text{pull}}=1.8\text{V}$ ,  $R_{\text{pull}}=10\text{k}\Omega$

1. Calculation of  $R_{\text{ON\_MAX}}$   
Calculated from the electrical characteristics based on  $V_{\text{RESETB}}/I_{\text{RBOUT\_MIN}}$   
 $R_{\text{ON\_MAX}} = 0.3\text{V} / 2.5\text{mA} \cong 120\Omega$  (MAX.)
2. Calculation of  $V_{\text{RESETB}}$   
Calculate the maximum value of the output "L" voltage using  $R_{\text{ON\_MAX}}$ .  
 $V_{\text{RESETB}} = V_{\text{pull}} / (1 + R_{\text{pull}} / R_{\text{ON\_MAX}}) = 1.8\text{V} / (1 + 10\text{k}\Omega / 120\Omega) \cong 21\text{mV}$

### 【Minimum value of output "H" voltage】

$$V_{\text{RESETB}} = V_{\text{pull}} - R_{\text{pull}} \times I_{\text{LEAKN\_MAX}}$$

$V_{\text{pull}}$  : minimum output "H" voltage

$I_{\text{LEAKN\_MAX}}$  : Leakage current maximum value of Nch driver M5.

Calculation Example)  $V_{\text{pull}}=6.0\text{V}$ ,  $R_{\text{pull}}=100\text{k}\Omega$  (\*2)

1. Calculation of  $I_{\text{LEAKN\_MAX}}$   
Calculated from the electrical characteristics based on  $I_{\text{LEAKN\_MAX}} = 0.1\mu\text{A}$  (MAX.)
2. Calculation of  $V_{\text{RESETB}}$   
Calculate the minimum value of the output "H" voltage using  $I_{\text{LEAKN\_MAX}}$ .  
 $V_{\text{RESETB}} = V_{\text{pull}} - R_{\text{pull}} \times I_{\text{LEAKN\_MAX}} = 6.0\text{V} - 100\text{k}\Omega \times 0.1\mu\text{A} = 5.99\text{V}$

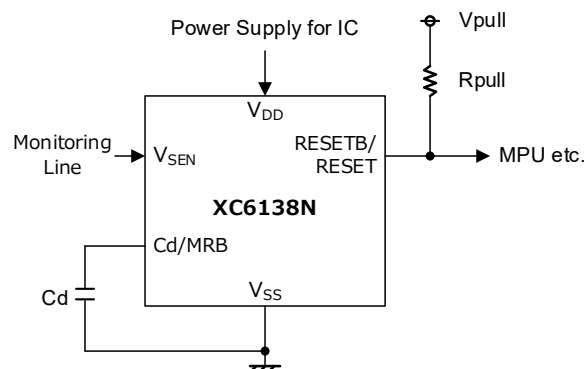


Fig. 6. Connection example of pull-up resistor (Nch Open Drain)



## ■ NOTES ON USE

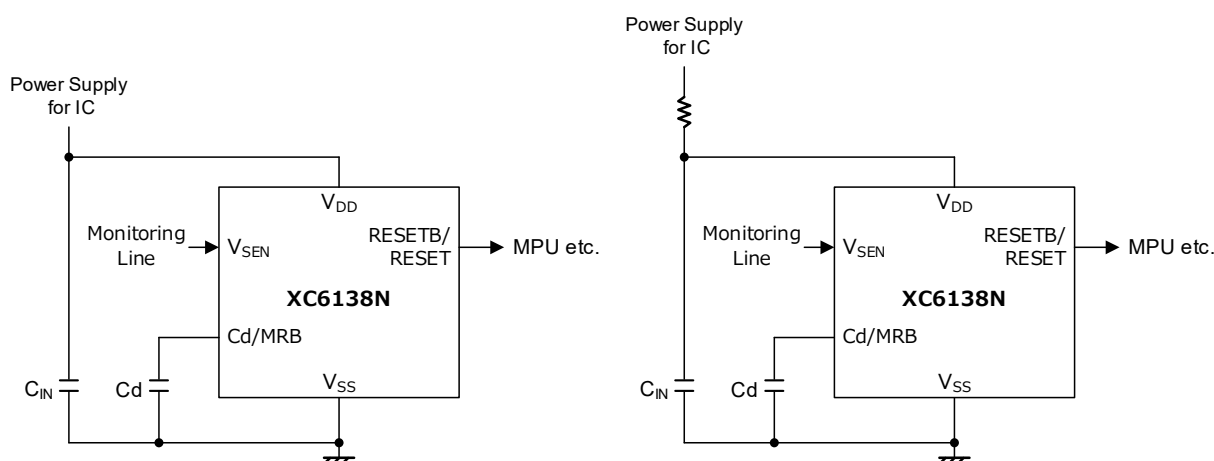
1) Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded. Also, if used under out of the recommended operating range, the IC may not operate normally or may cause deterioration.

2) When the  $V_{DD}$  pin voltage is lower than the operating voltage, the RESET/RESETB pin voltage becomes undefined regardless of the  $V_{SEN}$  pin voltage.

3) The following phenomena (a)~(b) may occur due to peripheral components, voltage fluctuations at  $V_{DD}$  pin, external noise, etc. If these phenomena occur, measures such as inserting a capacitor ( $C_{IN}$ ) between  $V_{DD}$  and  $V_{SS}$  may be necessary. (Please refer to the figure below for more details.)

(a) If a resistor ( $R_{IN}$ ) is inserted between the power supply and  $V_{DD}$  pin, the  $V_{DD}$  pin voltage drops due to the current flow and resistance ( $R_{IN}$ ) generated during detect and release. In addition, for CMOS output products, the drop in  $V_{DD}$  pin voltage becomes larger due to the output current. This temporary drop in  $V_{DD}$  pin voltage can cause output oscillation and malfunction.

(b) The power supply noise from external sources may cause malfunction.



4) If  $V_{DD}$  is started up with a voltage below the detection voltage applied to the  $V_{SEN}$  pin voltage, the output becomes undefined immediately after  $V_{DD}$  rises.

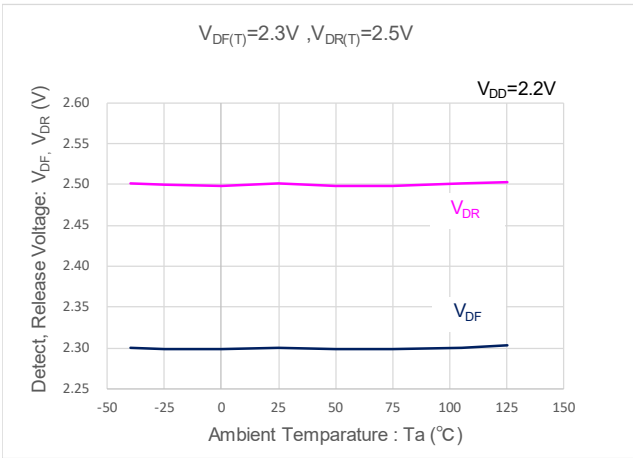
It is possible to suppress the unstable output immediately after the  $V_{DD}$  rises by connecting the delay capacitor  $C_d$  and releasing the set value of the delay time.

When taking countermeasures, adjust the delay capacitance  $C_d$  so that the release delay time is several milliseconds or longer. Otherwise please design the system/software structure for the output in order not to be undefined just after  $V_{DD}$  is raised.

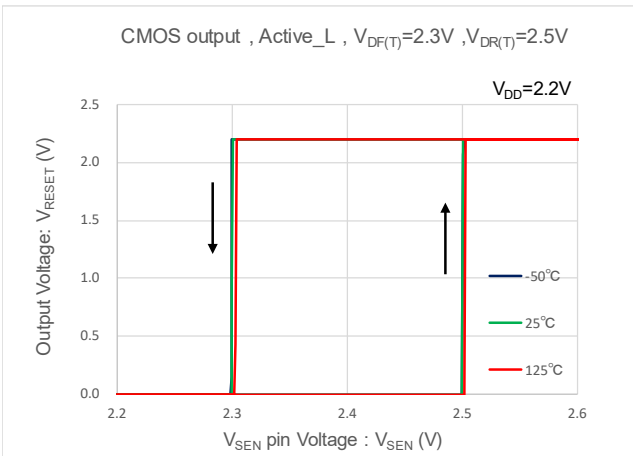
5) Torex places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

## TYPICAL PERFORMANCE CHARACTERISTICS

(1) Detect, Release Voltage vs Ambient Temperature

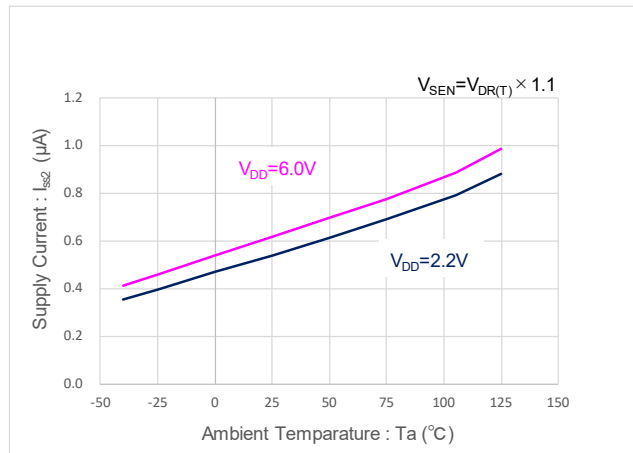
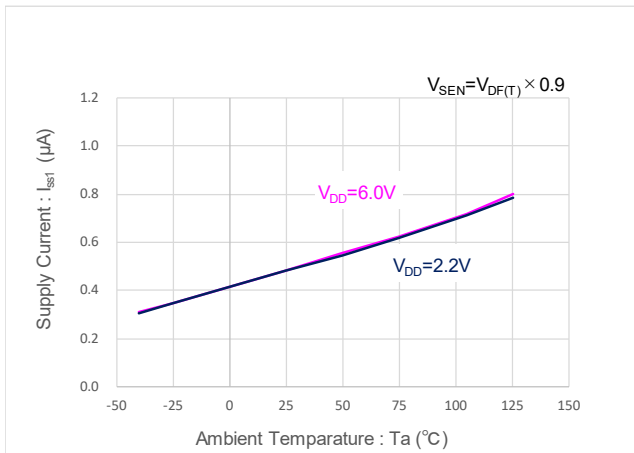


(2) Output Voltage vs SENSE Voltage

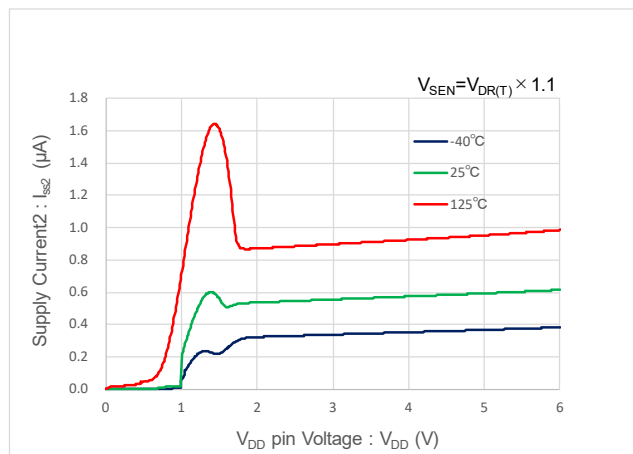
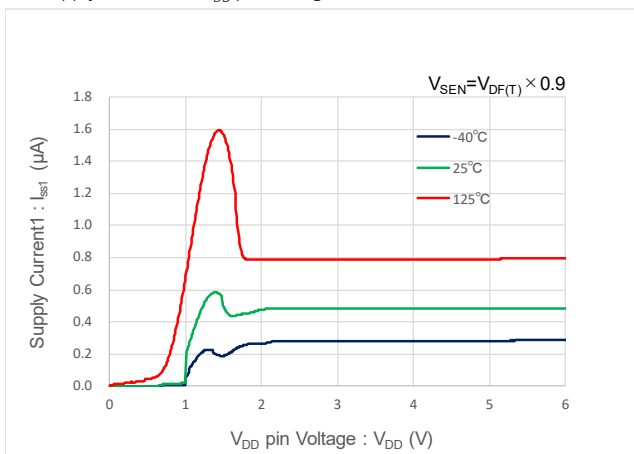


## TYPICAL PERFORMANCE CHARACTERISTICS

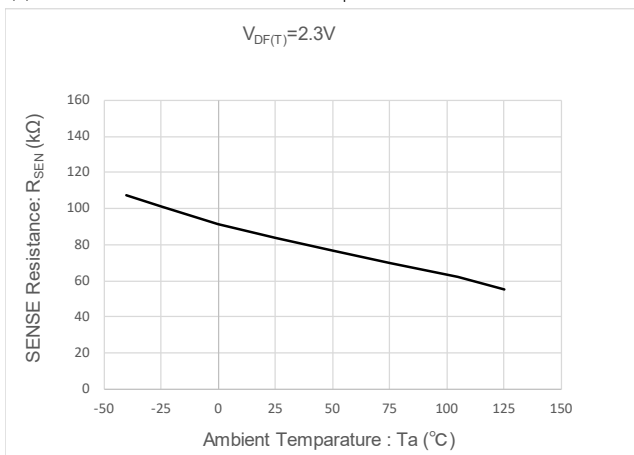
(3) Supply Current vs. Ambient Temperature



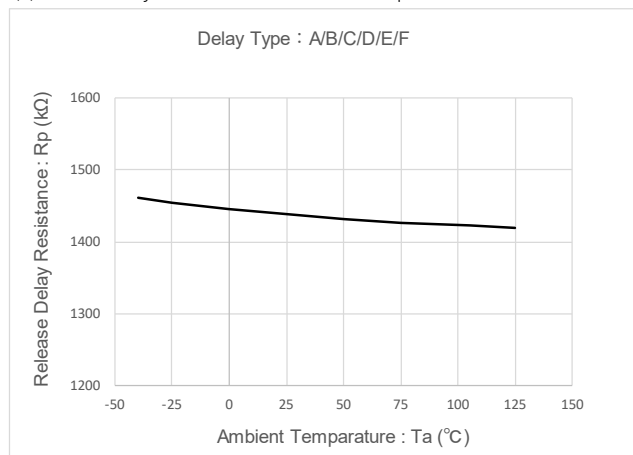
(4) Supply Current vs.  $V_{DD}$  pin Voltage



(5) SENSE Resistance vs Ambient Temperature

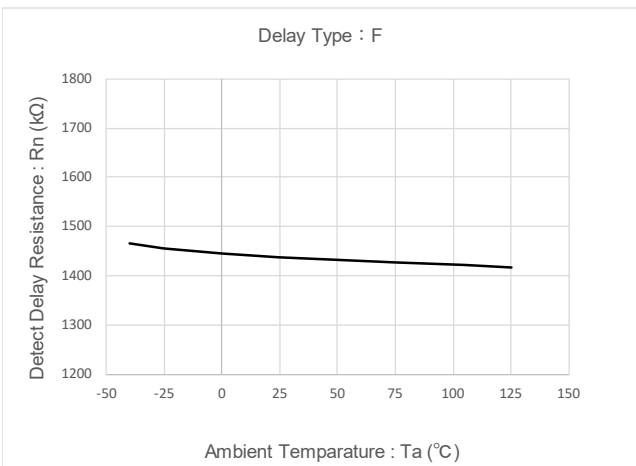
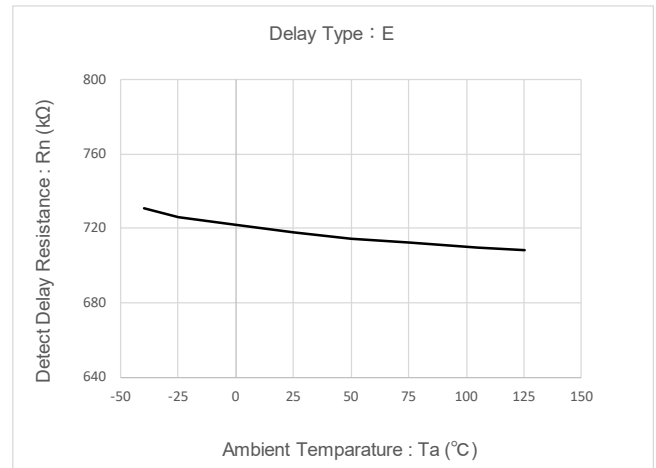
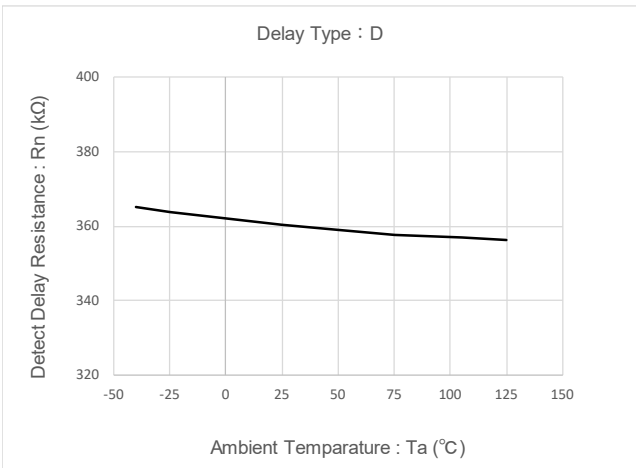
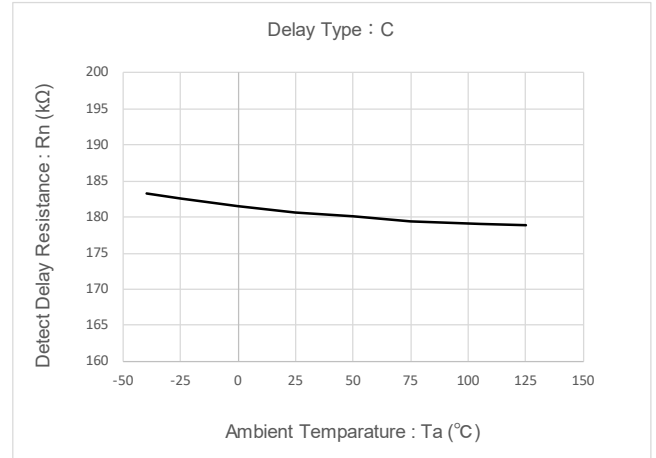
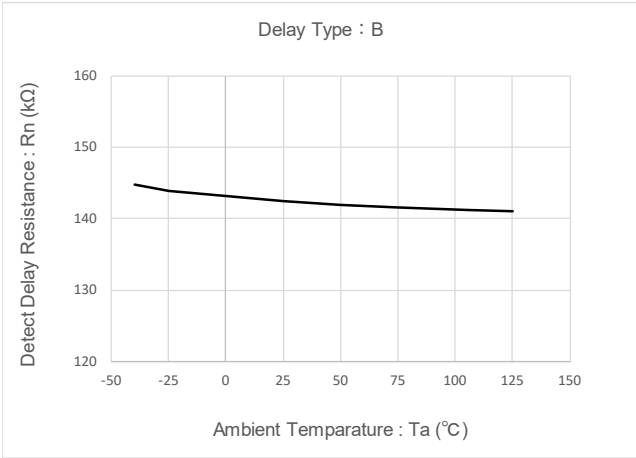


(6) Detect Delay Resistance vs Ambient Temperature



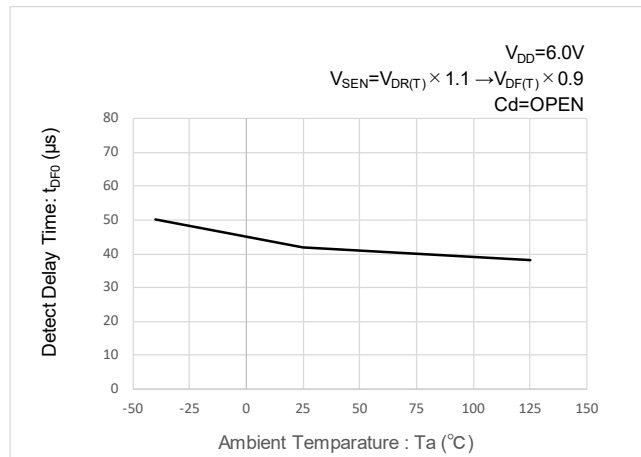
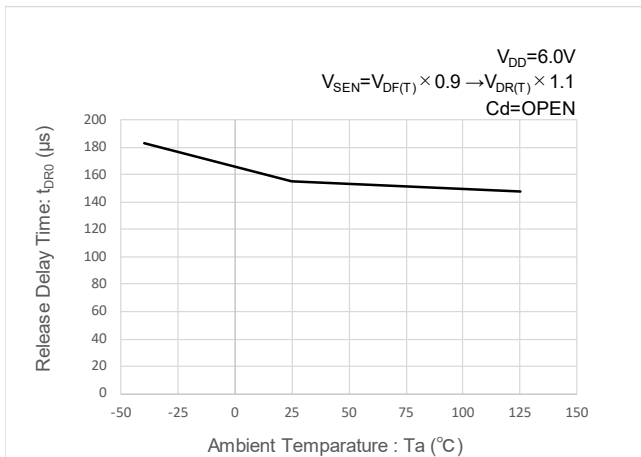
## TYPICAL PERFORMANCE CHARACTERISTICS

(7) Release Delay Resistance vs Ambient Temperature

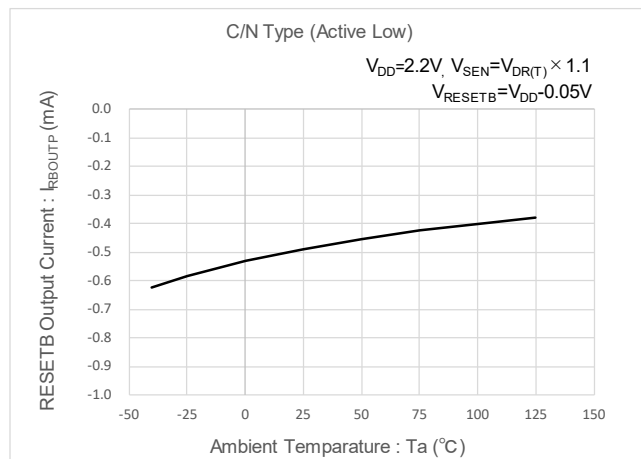
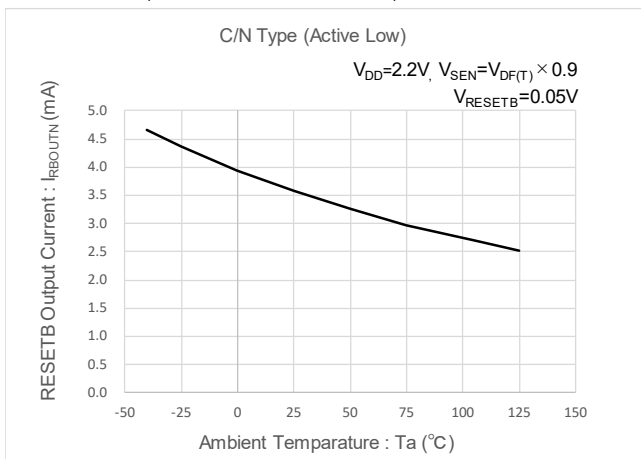


## TYPICAL PERFORMANCE CHARACTERISTICS

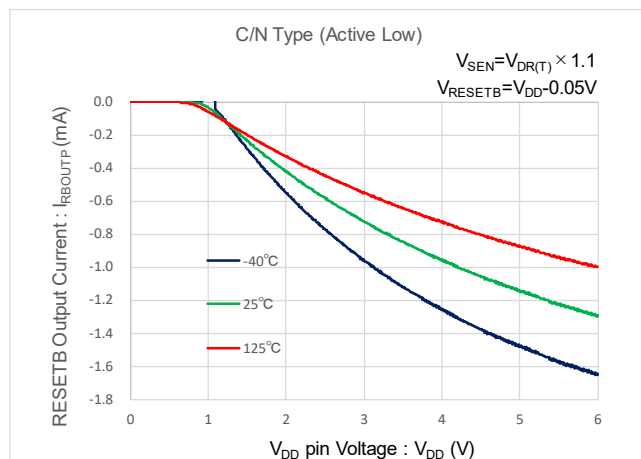
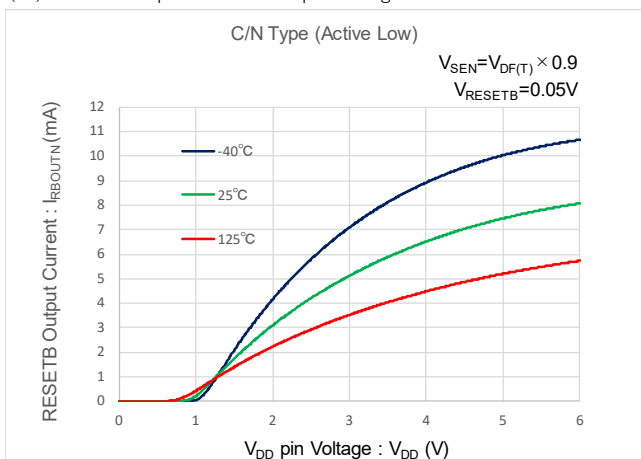
(8) Release/Detect Delay Time vs Ambient Temperature



(9) RESETB Output Current vs Ambient Temperature

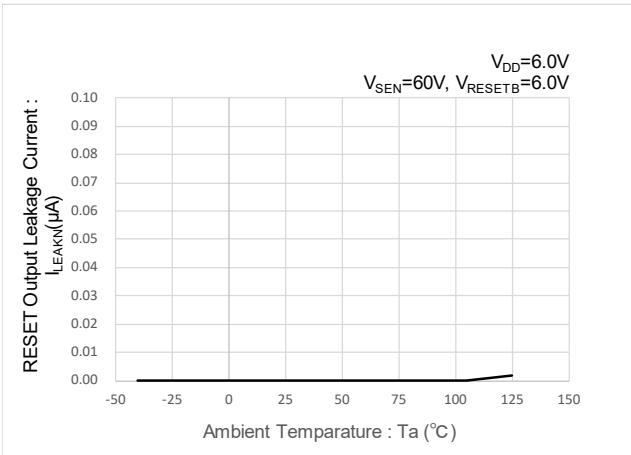


(10) RESETB Output Current vs Input Voltage

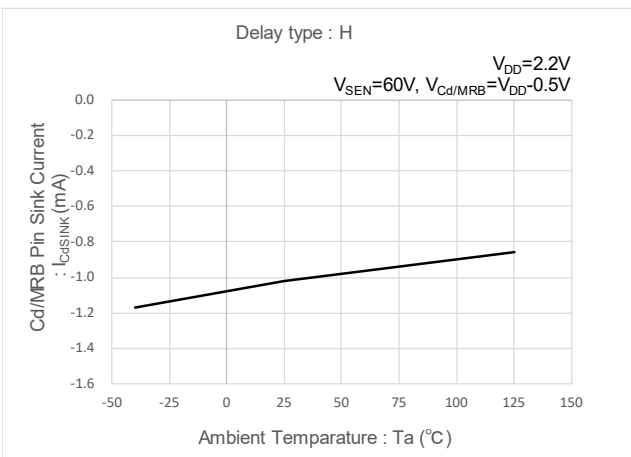


## TYPICAL PERFORMANCE CHARACTERISTICS

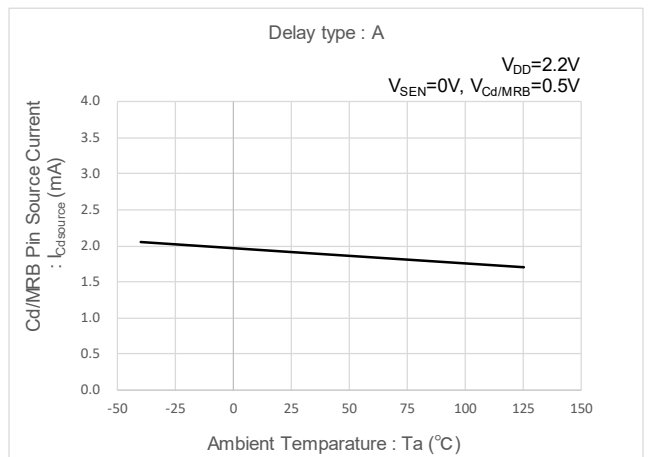
(11) RESET Output Leakage Current vs Ambient Temperature



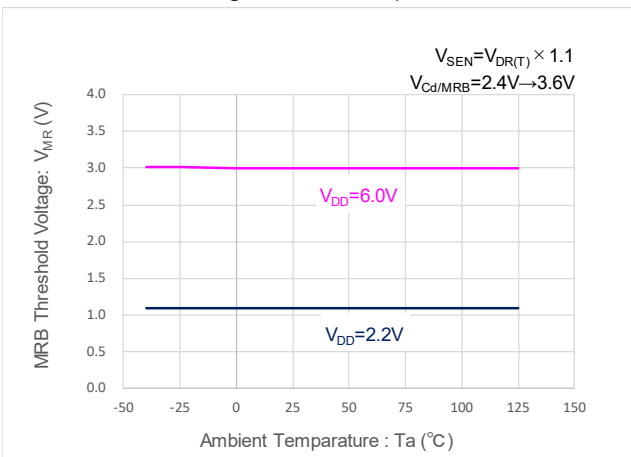
(12) Cd/MRB Pin Sink Current vs Ambient Temperature



(13) Cd/MRB Pin Source Current vs Ambient Temperature



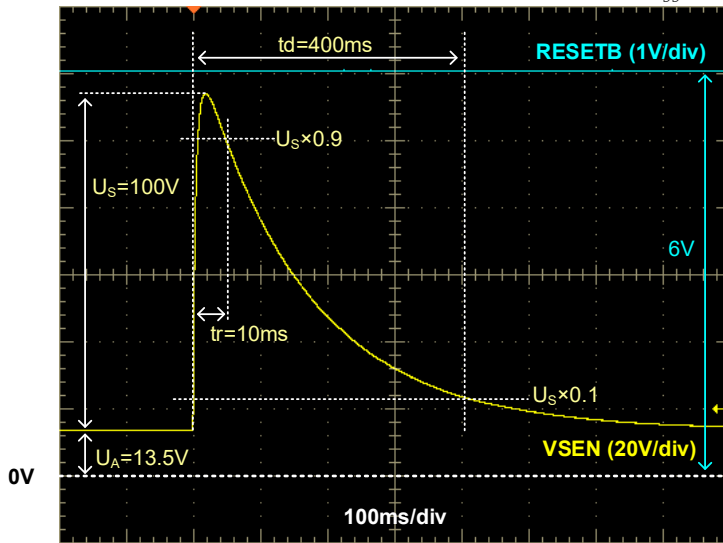
(14) MRB Threshold Voltage vs Ambient Temperature



## TYPICAL PERFORMANCE CHARACTERISTICS

(15) Load Dump

$V_{DF(T)}=6.0V / V_{DR(T)}=7.2V / \text{Active Low}$   
 $V_{DD} = 6V$



## ■ PACKAGING INFORMATION

For the latest package information go to, <http://www.torexsemi.com/technical-support/packages>

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
DFN1515-6A	<a href="#">DFN1515-6A PKG</a>	<a href="#">DFN1515-6A Power Dissipation</a>
SOT-25	<a href="#">SOT-25 PKG</a>	<a href="#">SOT-25 Power Dissipation</a>

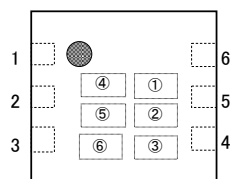


## MARKING RULE

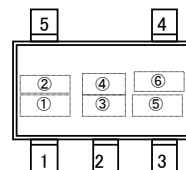
① represents product series

MARK	PRODUCT SERIES
0	XC6138*****-G

DFN1515-6A



SOT-25



②,③,④ represents internal sequential number

001~999、A01~A99、B01~B99、C01...Z99、AAA~AZZ、BAA~BZZ、CAA...ZZZ in order.

(G, I, J, O, Q, W excluded. No character inversion used.)

④,⑤ represents production lot number

01~09, 0A~0Z, 11~9Z, A1~A9, AA~AZ, B1~ZZ in order.

(G, I, J, O, Q, W excluded. No character inversion used.)

### ●Sequential number list

PRODUCT	②③④
XC6138 B H7D	001
XC6138 N A37	002
XC6138 N A94	003
XC6138 N AM1	004
XC6138 N AP0	005
XC6138 N APP	006
XC6138 N ANL	007
XC6138 N AN0	008
XC6138 N ARJ	009
XC6138 N CN0	010
XC6138 N CRJ	011
XC6138 N AL6	012
XC6138 C AN0	013
XC6138 C CN0	014
XC6138 C ARJ	015
XC6138 C CRJ	016
XC6138 N ARZ	017
XC6138 N APZ	018
XC6138 N APN	019
XC6138 N AQZ	020
XC6138 N AQT	021
XC6138 N ASY	022
XC6138 N AQE	023

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.
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