XC6121/XC6122
XC6123/XC6124 Series

ETR02009-012

Voltage Detector with Watchdog Function and ON/OFF Control (V_{DF}=1.6V~5.0V)

■GENERAL DESCRIPTION

The XC6121/XC6122/XC6123/XC6124 series is a group of high-precision, low current consumption voltage detectors with watchdog functions incorporating CMOS process technology. The series consist of a reference voltage source, delay circuit, comparator, and output driver. With the built-in delay circuit, the series do not require any external components to output signals with release delay time. The output type is V_{DFL} low when detected.

The EN/ENB pin can control ON and OFF of the watchdog functions. By setting the EN/ENB pin to low or high level, the watchdog function can be OFF while the voltage detector remains operation. Since the EN/ENB pin of the XC6122 and XC6124 series is internally pulled up to the V_{IN} pin or pulled down to the V_{SS} pin, these series can be used with the EN/ENB pin left open when the watchdog functions is used. The detect voltages are internally fixed 1.6V ~ 5.0V in increments of 0.1V, using laser trimming technology. Six watchdog timeout periods are available in a range from 50ms to 1.6s. Five release delay times are available in a range from 3.13ms to 400ms.

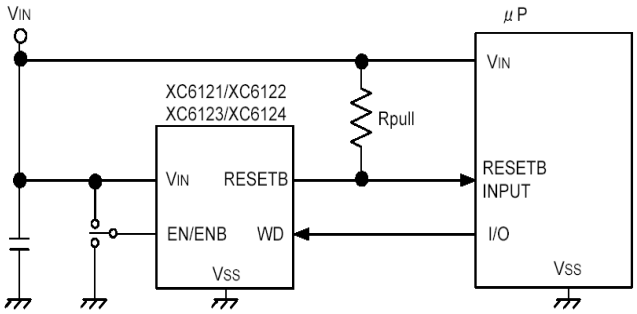
■APPLICATIONS

- Microprocessor watchdog monitoring and reset circuits
- Memory battery backup circuits
- System power-on reset circuits
- Power failure detection

■FEATURES

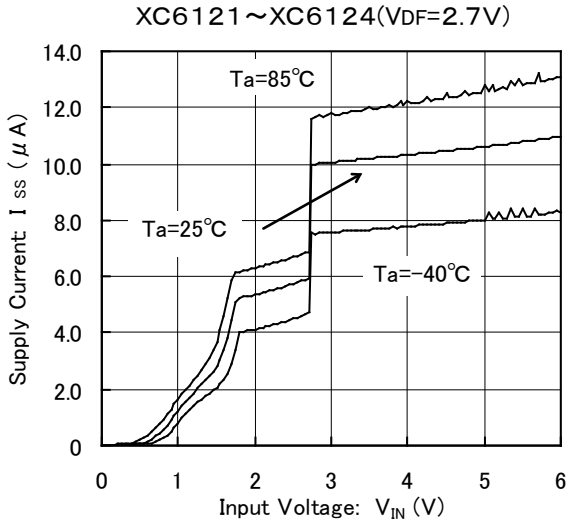
Detect Voltage Range	: 1.6V ~ 5.0V, ±2% (0.1V increments)
Hysteresis Width	: V_{DFL} x 5%
Operating Voltage Range	: 1.0V ~ 6.0V
Detect Voltage Temperature Characteristics	: ±100ppm/°C
Output Configuration	: N-channel open drain
Watchdog Pin	: Watchdog input If watchdog input maintains 'H' or 'L' within the watchdog timeout period, a reset signal is output from the RESETB pin.
EN/ENB Pin	: When the EN/ENB pin voltage is set to low or high level, the watchdog function is forced off.
Release Delay Time	: 400ms, 200ms, 100ms, 50ms, 3.13ms
Watchdog Timeout Period	: 1.6s, 800ms, 400ms, 200ms, 100ms, 50ms
Operating Ambient Temperature	: -40°C~ 85°C
Packages	: SOT-25, USP-6C
Environmentally Friendly	: EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT

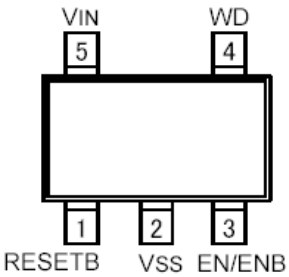


■TYPICAL PERFORMANCE CHARACTERISTICS

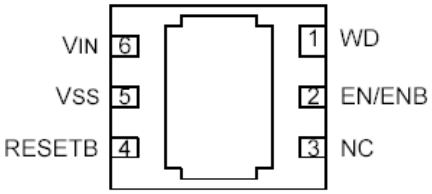
●Supply Current vs. Input Voltage



■PIN CONFIGURATION



SOT-25
(TOP VIEW)



USP-6C
(BOTTOM VIEW)

* The dissipation pad for the USP-6C package should be solder-plated in reference mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the Vss (No. 5) pin.

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-25	USP-6C		
1	4	RESETB	Reset Output
2	5	V_{SS}	Ground
3	2	EN/ENB	Watchdog ON/OFF Control
4	1	WD	Watchdog
5	6	V_{IN}	Power Input
-	3	NC	No Connection

■PRODUCT CLASSIFICATION

●Selection Guide

SERIES	RESETB OUTPUT	HYSTERESIS	EN/ENB PIN FUNCTION	
			EN/ENB Input Logic (*2)	Pull-up or Pull-down Resistor
XC6121	Active Low	VDFL×5%	EN	Without Pull-up Resistor
XC6122			EN	With Pull-up Resistor
XC6123			ENB	Without Pull-down Resistor
XC6124			ENB	With Pull-down Resistor

(*1) The output type of RESETB is set to L level at the time of detection.

(*2) EN input logic: The watchdog function turns on when the EN pin becomes high level.
ENB input logic: The watchdog function turns on when the ENB pin becomes low level.

●Ordering Information

XC6121①②③④⑤⑥−⑦(*2): EN Pin: No Pull-Up Resistor
XC6122①②③④⑤⑥−⑦(*2): EN Pin: Pull-Up Resistor
XC6123①②③④⑤⑥−⑦(*2): ENB Pin: No Pull-Down Resistor
XC6124①②③④⑤⑥−⑦(*2): ENB Pin: Pull-Down Resistor

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Release Delay Time(*1)	A	3.13ms
		C	50ms
		D	100ms
		E	200ms
		F	400ms
②	Watchdog Timeout Period	2	50ms
		3	100ms
		4	200ms
		5	400ms
		6	1.6s
		7	800ms
③④	Detect Voltage	16 ~ 50	Detect voltage ex.) 4.5V: ③⇒4, ④⇒5
⑤⑥−⑦(*2)	Packages (Order Unit)	MR-G	SOT-25 (3,000pcs/Reel)
		ER-G	USP-6C (3,000pcs/Reel)

(*1) Please set the release delay time shorter than or equal to the watchdog timeout period.
ex.) XC6121D327MR-G or XC6121D627MR-G

(*2) The “-G” suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

■PIN LOGIC CONDITIONS

PIN NAME	LOGIC	CONDITIONS
V_{IN}	H	$V_{IN} \geqq V_{DFL}+V_{HYS}$
	L	$V_{IN} \leqq V_{DFL}$
EN/ENB	H	$V_{EN}/V_{ENB} \geqq 1.30V$
	L	$V_{EN}/V_{ENB} \leqq 0.35V$
WD	H	The state maintaining $WD \geqq V_{WDH}$ for more than t_{WD}
	L	The state maintaining $WD \leqq V_{WDL}$ for more than t_{WD}
	L→H	$V_{WDL} \rightarrow V_{WDH}$, $300ns \leqq t_{WDIN} \leqq t_{WD}$
	H→L	$V_{WDH} \rightarrow V_{WDL}$, $300ns \leqq t_{WDIN} \leqq t_{WD}$

NOTE:
V_{DFL}: Detect Voltage
V_{HYS}: Hysteresis Range
V_{WDH}: WD High Level Voltage
V_{WDL}: WD Low Level Voltage
t_{WDIN}: WD Pulse Width
t_{WD}: WD Timeout Period
For the details of each parameter, please see the electrical characteristics.

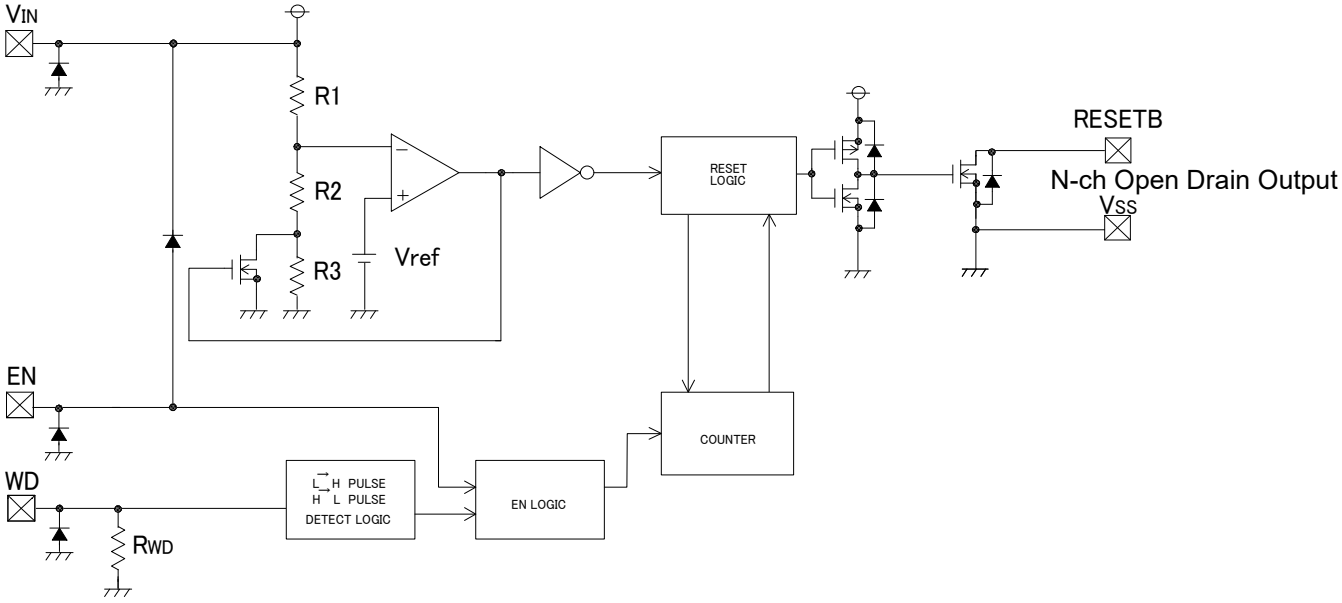
■FUNCTION CHART

V_{IN}	XC6121/XC6122	XC6123/XC6124	V_{WD}	V_{RESETB} (*2)
	V_{EN}	V_{ENB}		
H	H	L	H	Repeating detect and release (H→L→H)
			L	
			OPEN	
			L⇔H	H
H	L	H	*1	H
L		L		L

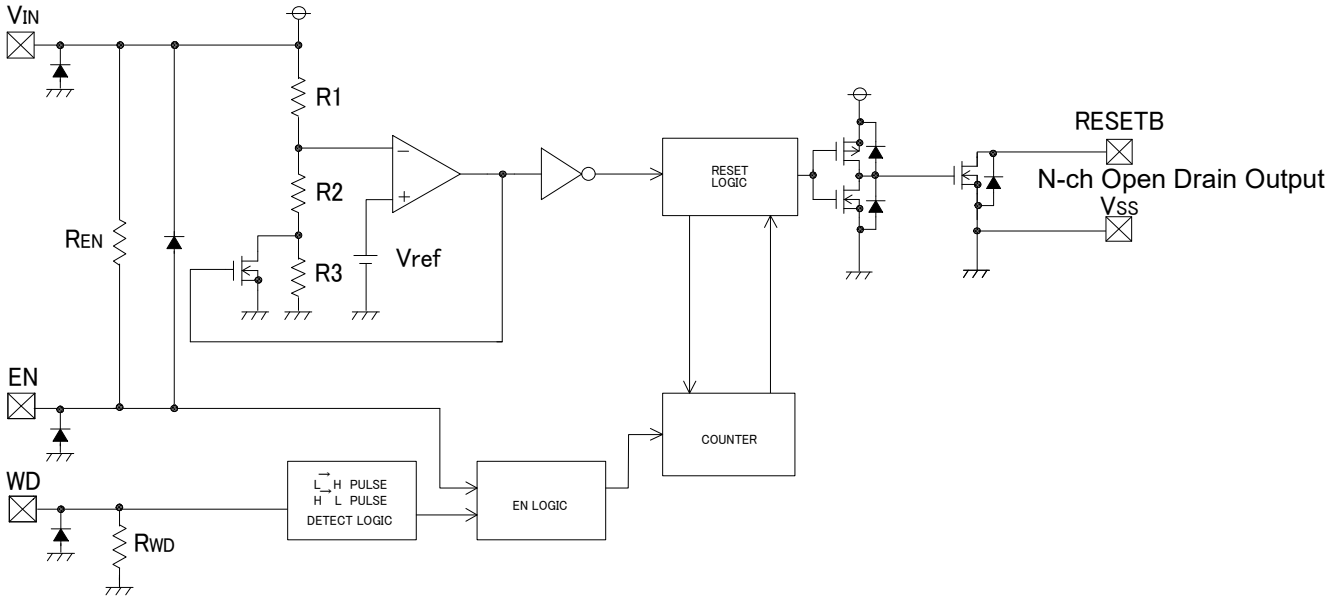
NOTE:
*1: Including all logics of the WD (V_{WD}=H, L, OPEN, H→L, L→H).
*2: When the V_{RESETB} is High, the circuit is in the release state.
When the V_{RESETB} is Low, the circuit is in the detection state.
*3: V_{IN}=L and V_{EN}/V_{ENB}=H can not be combined because the rated input voltage of the EN/ENB pin is Vss-0.3V to V_{IN}+0.3V.
*4: The RESETB pin becomes indefinite operation while $0.35V<V_{EN}/V_{ENB}<1.3V$.
*5: The EN pin of the XC6121 series is not internally pulled up. When using the watchdog function, please drive the V_{EN} pin in high level.
The EN pin of the XC6122 series is internally pulled up. The watchdog function can be used even the EN pin left open.
The ENB pin of the XC6123 series is not internally pulled down. When using the watchdog function, please drive the V_{ENB} pin in low level.
The ENB pin of the XC6124 series is internally pulled down. The watchdog function can be used even the ENB pin left open.

■BLOCK DIAGRAMS

●XC6121 Series

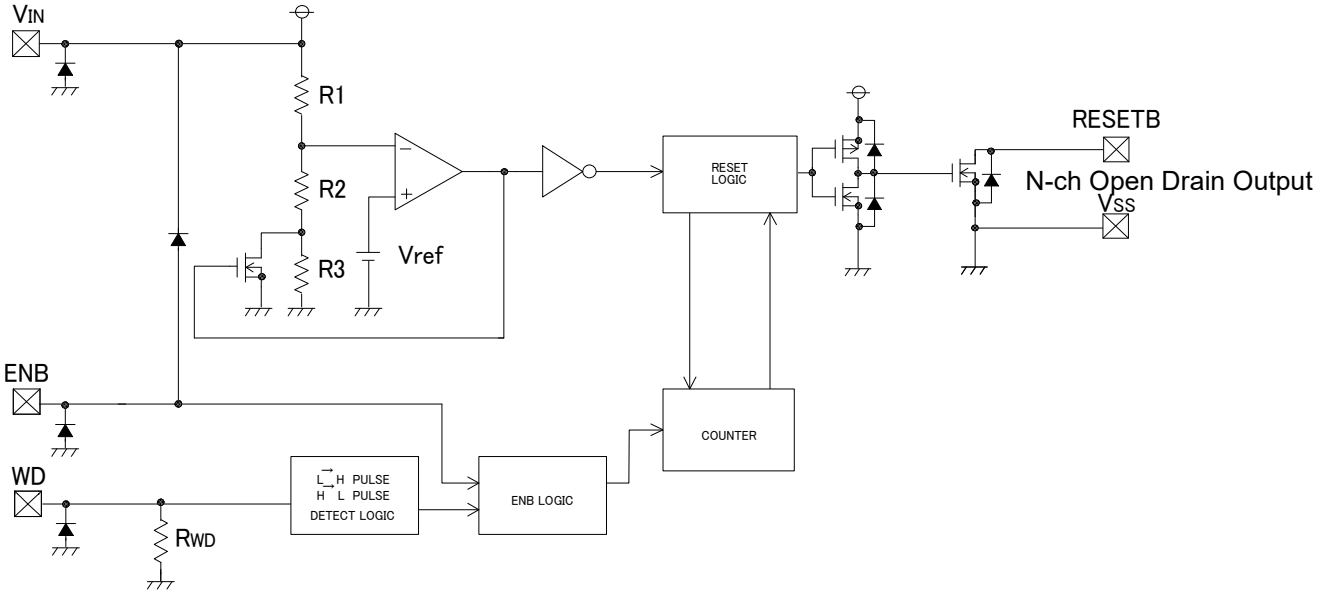


●XC6122 Series

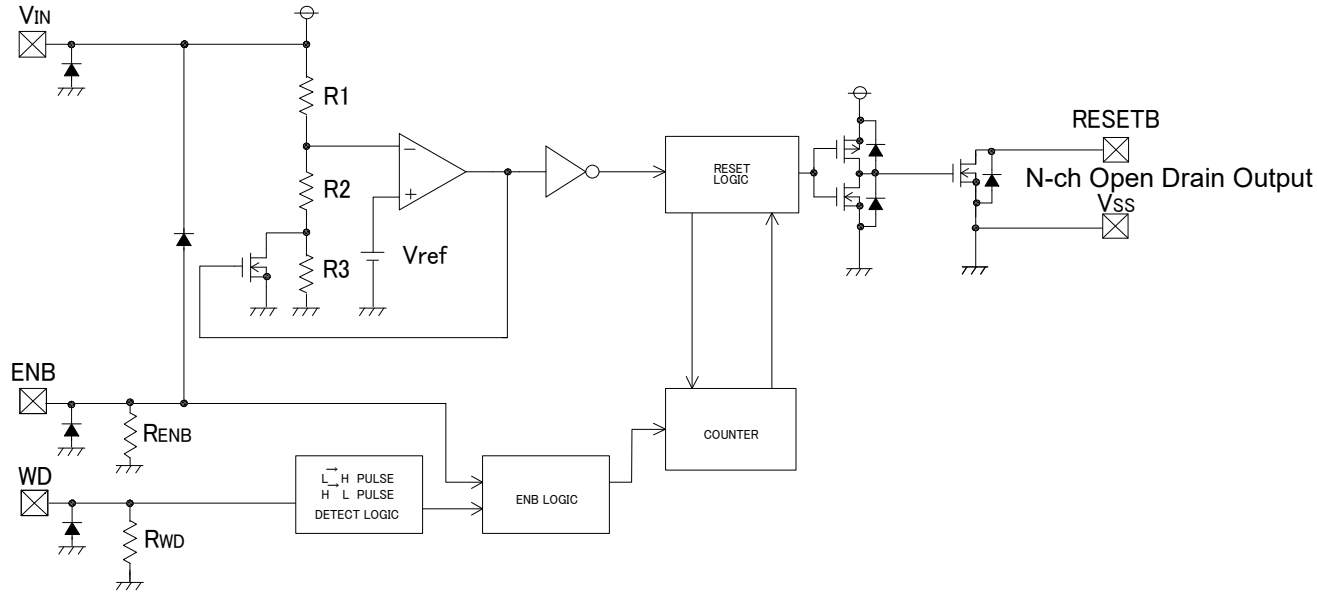


■BLOCK DIAGRAMS (Continued)

●XC6123 Series



●XC6124 Series



■ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	V_{SS} -0.3 ~ 7.0	V
		V_{EN}/V_{ENB}	V_{SS}-0.3 ~ V_{IN}+0.3≦7.0	
		V_{WD}	V_{SS} -0.3 ~ 7.0	
Output Current		I_{RBOUT}	20	mA
Output Voltage		V_{RESETB}	V_{SS} -0.3 ~ 7.0	V
Power Dissipation (Ta=25℃)	SOT-25	Pd	250	mW
	USP-6C		120	
Operating Ambient Temperature		Topr	-40 ~ 85	ºC
Storage Temperature		Tstg	-55 ~ 125	ºC

■ELECTRICAL CHARACTERISTICS

Ta=25 °C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Detect Voltage	V_{DFL}	V_{EN}=V_{SS}	$V_{DFL(T)}$ × 0.98	$V_{DFL(T)}$	$V_{DFL(T)}$ × 1.02	V	①
Hysteresis Width	V_{HYS}	V_{EN}=V_{SS}	V_{DFL} × 0.02	V_{DFL} × 0.05	V_{DFL} × 0.08	V	①
Supply Current (*1)	I_{SS}	WD=OPEN, V_{IN}=$V_{DFL(T)}$×0.9	-	5	11	µA	②
		WD=OPEN, V_{IN}=$V_{DFL(T)}$×1.1	-	10	16		
		WD=OPEN, V_{IN}=6.0V	-	12	18		
Operating Voltage	V_{IN}		1.0	-	6.0	V	①
Output Current	I_{RBOUT}	N-ch. V_{DS}=0.5V, V_{IN}=1.0V	0.15	0.5	-	mA	③
		N-ch. V_{DS}=0.5V, V_{IN}=2.0V ($V_{DFL(T)}$> 2.0V)	2.0	2.5	-		
		N-ch. V_{DS}=0.5V, V_{IN}=3.0V ($V_{DFL(T)}$ >3.0V)	3.0	3.5	-		
		N-ch. V_{DS}=0.5V, V_{IN}=4.0V ($V_{DFL(T)}$ >4.0V)	3.5	4.0	-		
Temperature Characteristics	$\triangle V_{DFL}$ / $\triangle$Topr・V_{DFL}	-40°C ≦ Topr ≦ 85 °C	-	±100	-	ppm/ °C	①
Release Delay Time (V_{DFL}≦1.8V)	t_{DR}	Time until V_{IN} is increased from 1.0V to 2.0V and attains to the release time level, and the Reset output pin releases.	2.00	3.13	5.00	ms	④
			37	50	63		
			75	100	125		
			150	200	250		
			300	400	500		
Release Delay Time (V_{DFL}≧1.9V)	t_{DR}	Time until V_{IN} is increased from 1.0V to (V_{DFL} x 1.1) and attains to the release time level, and the Reset output pin releases.	2.00	3.13	5.00	ms	④
			37	50	63		
			75	100	125		
			150	200	250		
			300	400	500		
Detect Delay Time	t_{DF}	Time until V_{IN} is decreased from 6.0V to 1.0V and attains to the detect voltage level, and the Reset output pin detects while the WD pin left open.	-	5.5	33	µs	④
V_{DFL} Leakage Current	I_{LEAK}	V_{IN}=6.0V, V_{RESETB}=6.0V	-	0.01	0.1	µA	③
Watchdog Timeout Period (V_{DFL}≦1.8V)	t_{WD}	Time until V_{IN} increases form 1.0V to 2.0V and the Reset output pin is released to go into the detection state. (WD=OPEN)	37	50	63	ms	⑤
			75	100	125		
			150	200	250		
			300	400	500		
			600	800	1000		
			1200	1600	2000		
Watchdog Timeout Period (V_{DFL}≧1.9V)	t_{WD}	Time until V_{IN} increases from 1.0V to (V_{DFL} x 1.1) and the Reset output pin is released to go into the detection state. (WD=OPEN)	37	50	63	ms	⑤
			75	100	125		
			150	200	250		
			300	400	500		
			600	800	1000		
			1200	1600	2000		

■ELECTRICAL CHARACTERISTICS (Continued)

Ta=25 °C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Watchdog Minimum Pulse Width	tWDIN	VIN=6.0V, Apply pulse from 6.0V to 0V to the WD pin.	300	-	-	ns	⑥
Watchdog High Level Voltage	VWDH	VIN=VDFL x 1.1 ~ 6.0V	VIN x 0.7	-	6	V	⑥
Watchdog Low Level Voltage	VWDL	VIN=VDFL x 1.1 ~ 6.0V	0	-	VIN x 0.3	V	⑥
Watchdog Pull-down Resistance	RWD	VWD=6V, RWD=VWD/IWD	300	600	900	kΩ	⑦
EN/ENB High Level Voltage	VENH/VENBH	VIN=VDFL x 1.1 ~ 6.0V	1.3	-	VIN	V	⑧
EN/ENB Low Level Voltage	VENL/VENBL	VIN=VDFL x 1.1 ~ 6.0V	0	-	0.35	V	⑧
EN Pull-up Resistance (*2)	REN	VIN=6.0V, VEN=0V, REN=VIN / IEN	1.0	1.6	2.4	MΩ	⑨
ENB Pull-down Resistance (*3)	RENB	VIN=6.0V, VENB=6V, RENB=VENB / IENB					

NOTE:

* In case where no EN/ENB pin's condition written in the test condition field, $V_{EN}=V_{IN}$ and $V_{ENB}=V_{SS}$.

** $V_{DFL(T)}$=Setting detect voltage value

(*1) The condition when the watchdog pin is ON.
The EN/ENB pin is CMOS input. For the XC6122 (pull-up resistor) and XC6124 (pull-down resistor), supply current increases in the following values when the watchdog function is OFF.
XC6122 Series : (VIN-VEHL)/1.6MΩ(TYP.)
XC6124 Series : VEHBH/1.6MΩ(TYP.)

(*2) For the XC6122 series only.

(*3) For the XC6124 series only.

■OPERATIONAL EXPLANATION

The XC6121/6122/6123/6124 series compare, using the error amplifier, the voltage of the internal voltage reference source with the voltage divided by R1, R2 and R3 connected to the V_{IN} pin. The resulting output signal from the error amplifier activates the watchdog logic, delay circuit and the output driver. When the V_{IN} pin voltage gradually falls and finally reaches the detect voltage, the RESETB pin output goes from high to low in the case of the V_{DFL} type ICs.

<RESETB / RESET Pin Output Signal>

* V_{DFL} (RESETB) type - output signal: Low when detected.

The RESETB pin output goes from high to low whenever the V_{IN} pin voltage falls below the detect voltage. The RESETB pin remains low for the release delay time (t_{DR}) after the V_{IN} pin voltage reaches the release voltage. If neither rising nor falling signals are applied to the WD pin within the watchdog timeout period, the RESETB pin output remains low for the release delay time (t_{DR}), and thereafter the RESET pin outputs high level signal.

<Hysteresis>

When the internal comparator output is high, the NMOS transistor connected in parallel to R3 is turned ON, activating the hysteresis circuit. The difference between the release and detect voltages represents the hysteresis width, as shown by the following calculations:

V_{DFL} (detect voltage) = (R1+R2+R3) x Vref / (R2+R3)
V_{DR} (release voltage) = (R1+R2) x Vref / (R2)
V_{HYS} (hysteresis width) =V_{DR}-V_{DFL} (V)
V_{DR} > V_{DFL}
* Please refer to the block diagrams for R1, R2, R3 and Vref.
* Hysteresis width is selectable from V_{DFL} x 0.05 (TYP.).

<Watchdog (WD) Pin>

The series use a watchdog timer to detect malfunction or “runaway” of the microprocessor. If neither rising nor falling signals are applied from the microprocessor within the watchdog timeout period, the reset signal is output. The RESETB pin output maintains the detection state for the release delay time (t_{DR}), and thereafter the RESETB pin outputs low to high signal.

The watchdog pin is pulled down to the V_{SS} internally. When the watchdog pin is not connected, A reset signal comes out after the watchdog timeout period. Six watchdog timeout period settings (t_{WD}) are available in 1.6s, 800ms, 400ms, 200ms, 100ms, and 50ms.

■OPERATIONAL EXPLANATION

<EN Pin>

In case where the watchdog function is not used, When the EN pin input driven to low level, only the watchdog function is forced off while the detect voltage circuit remains operation. For using the watchdog function, the EN pin should be used in high level. Even after the input voltage and the EN pin voltage are driven back high, the RESETB pin output maintains the detection state for the release delay time (T_{DR}). (Refer to the TIMING CHART 1-①.)

During the release delay time, if the EN pin voltage is changed from the "L" to the "H" level, the release delay time is reset and the release delay time count resumes.
(Refer to the TIMING CHART 1-③.)

The watchdog function recovers immediately when the input voltage becomes higher than the release voltage and the EN pin voltage driven from low to high level. (Refer to the TIMING CHART 1-②.)

A diode, which is an input protection element, is connected between the EN pin and V_{IN} pin. Therefore, if the EN pin is applied voltage that exceeds V_{IN}, the current will flow to V_{IN} through the diode. For avoiding any damage to the IC, please use this IC within the stated maximum ratings (V_{SS} -0.3V ~ V_{IN} +0.3V) on the EN pin.

<ENB Pin>

In case where the watchdog function is not used, when the ENB pin input driven to high level, only the watchdog function is forced off while the detect voltage circuit remains operation. For using the watchdog function, the ENB pin should be used in low level. Even after the input voltage and the ENB pin voltage are driven back low, the RESETB pin output maintains the detection state for the release delay time (t_{DR}). (Refer to the TIMING CHART 2-①.)

During the release delay time, if the EN pin voltage is changed from the "H" to the "L" level, the release delay time is reset and the release delay time count resumes.
(Refer to the TIMING CHART 2-③.)

The watchdog function recovers immediately when the input voltage becomes higher than the release voltage and the ENB pin voltage driven from high to low level. (Refer to the TIMING CHART 2-②.)

A diode, which is an input protection element, is connected between the ENB pin and V_{IN} pin. Therefore, if the ENB pin is applied voltage that exceeds V_{IN}, the current will flow to V_{IN} through the diode. For avoiding any damage to the IC, please use this IC within the stated maximum ratings (V_{SS} -0.3V ~ V_{IN} +0.3V) on the ENB pin.

<Release Delay Time>

The Release delay time (t_{DR}) is the time until the V_{IN} pin voltage reach the release voltage and the device to enter the released state. The release delay time (t_{DR}) is the time until the internal watchdog timer to restart if no rising or falling signal is input to the WD pin within the watchdog timeout period. Five release delay time (t_{DR}) watchdog timeout period settings are available in 400ms, 200ms, 100ms, 50ms, and 3.13ms.

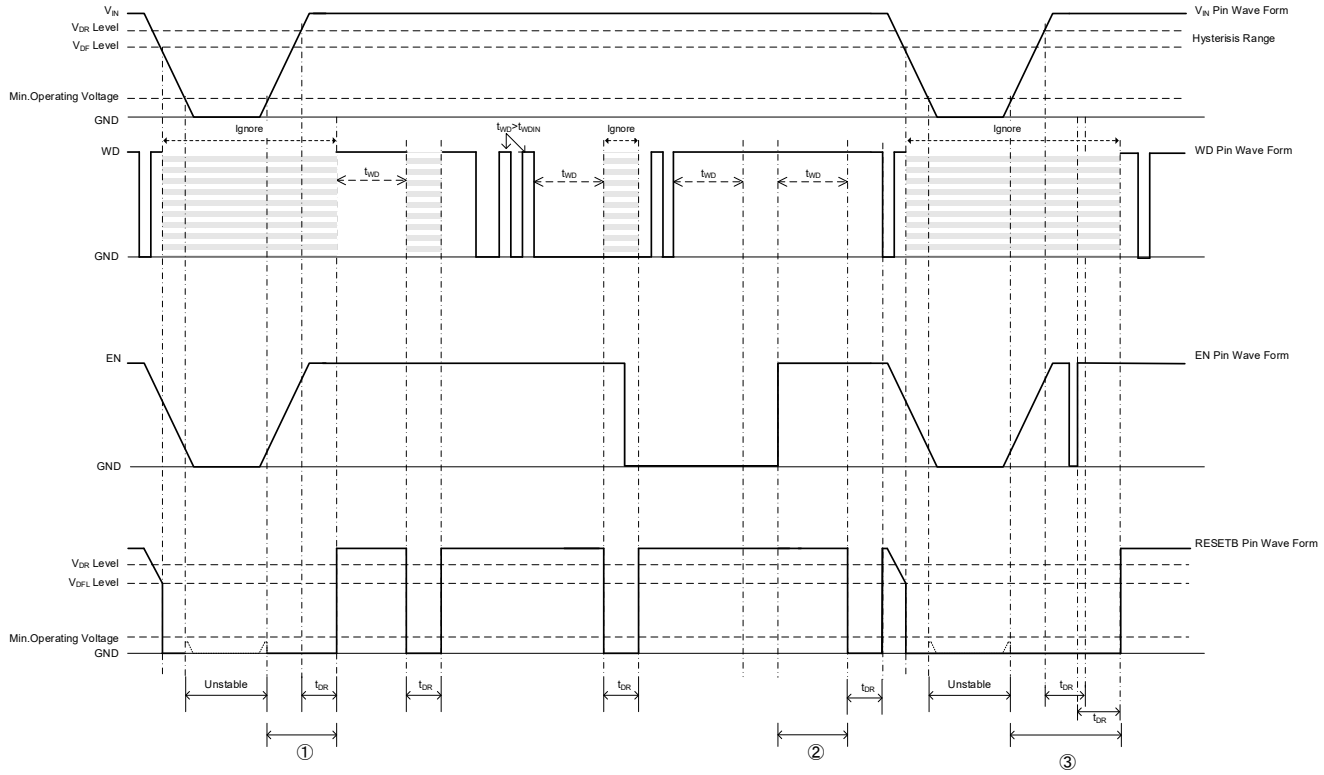
<Detect Delay Time>

Detect Delay Time (t_{DF}) is the time that elapses from when the V_{IN} pin voltage falls to the detect voltage until the RESETB pin output goes into the detection state.

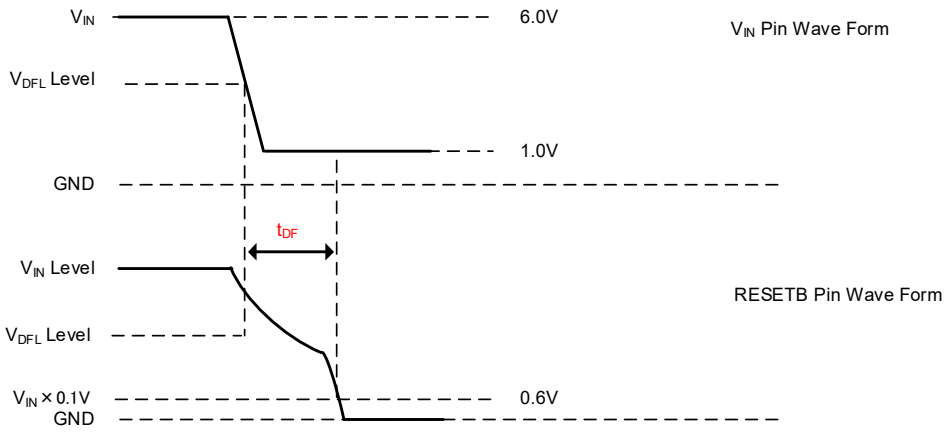
■TIMING CHARTS

1. XC6121/XC6122 Series (EN products)

●N-ch Open Drain Output (Rpull=100kΩ)



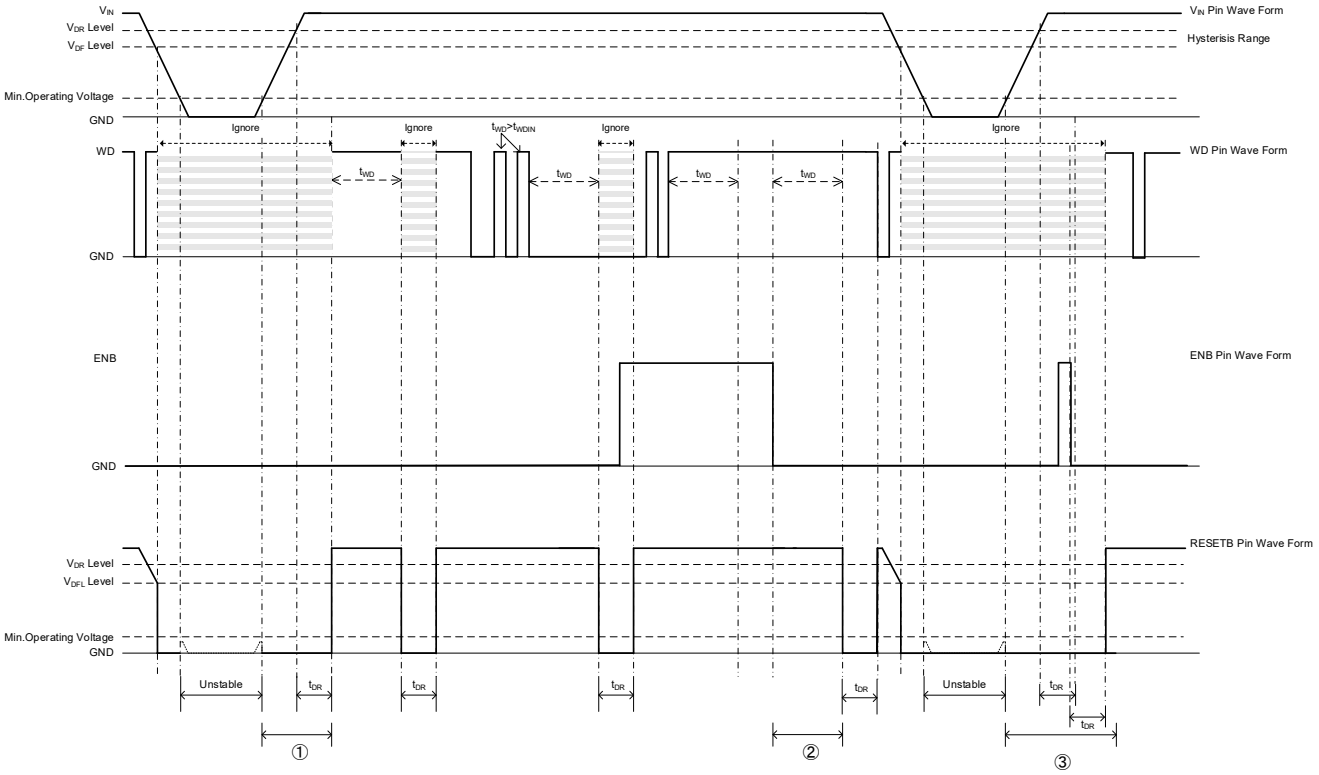
*Detect Delay time(t_{DF})



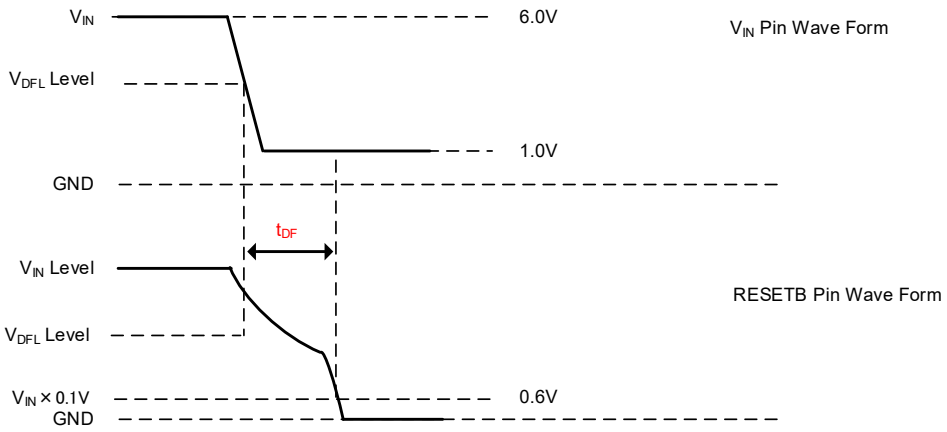
■TIMING CHARTS (Continued)

2. XC6123/XC6124 Series (ENB products)

●N-ch Open Drain Output (Rpull=100kΩ)



*Detect Delay time(t_{DF})



■NOTES ON USE

1. Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

2. When a resistor is connected between the V_{IN} pin and the input, the V_{IN} voltage drops while the IC is operating and a malfunction may occur as a result of the IC's through current.

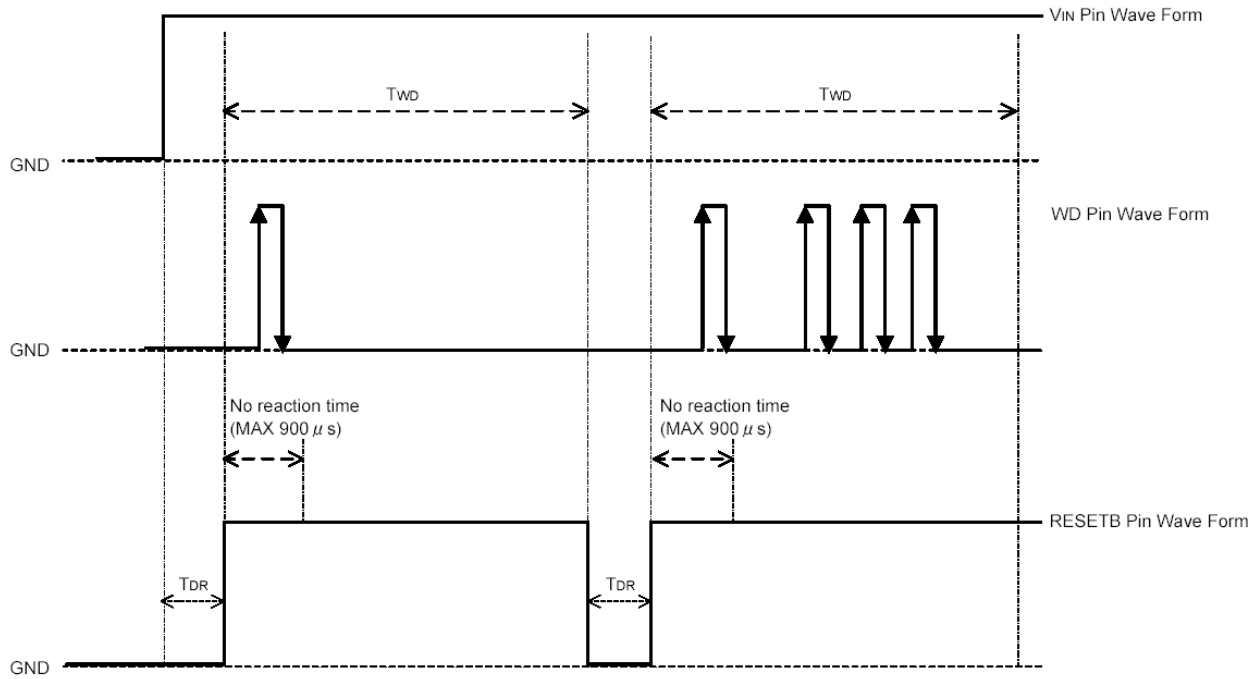
3. In order to stabilize the IC's operations, please ensure that the V_{IN} pin's input frequency's rise and fall times are more than 1μs/V.

4. Noise at the power supply may cause a malfunction of the watchdog operation or the voltage detector. In such case, please strength V_{IN} and GND lines. Also, please connect a capacitor such as 0.22μF between the V_{IN} pin and the GND pin and evaluate the device on the actual board carefully before use.

5. Protecting against a malfunction while the watchdog time out period, an ignoring time (no reaction time) occurs to the rise and fall times. Referring to the figure below, the ignoring time (no reaction time) lasts for 900μs at maximum.
(refer to the Figure1 below)

6. The EN pin of the XC6121 series is not internally pulled up. When using the watchdog function, please drive the V_{EN} pin in high level. The EN pin of the XC6122 series is internally pulled up. The watchdog function can be used even the EN pin left open. The ENB pin of the XC6123 series is not internally pulled down. When using the watchdog function, please drive the V_{ENB} pin in low level. The ENB pin of the XC6124 series is internally pulled down. The watchdog function can be used even the ENB pin left open.

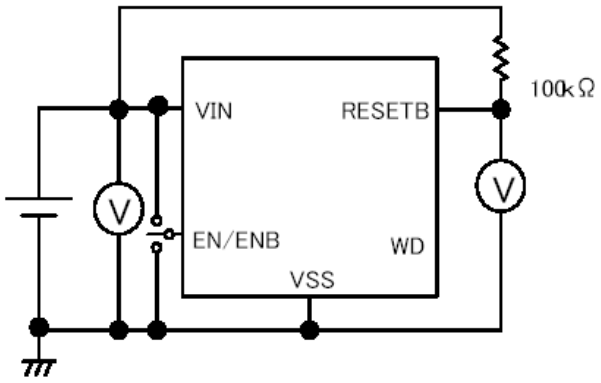
7. Torex places an importance on improving our products and its reliability.
However, by any possibility, we would request user fail-safe design and post-aging treatment on system or equipment.



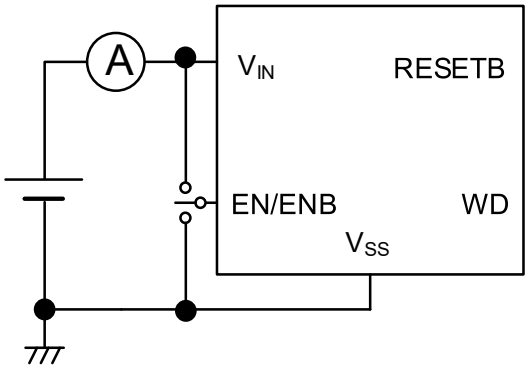
[Figure1]

■TEST CIRCUITS

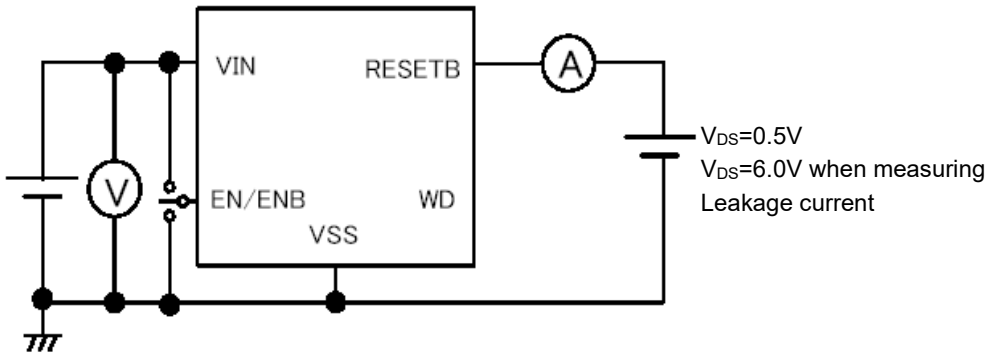
Circuit ①



Circuit ②

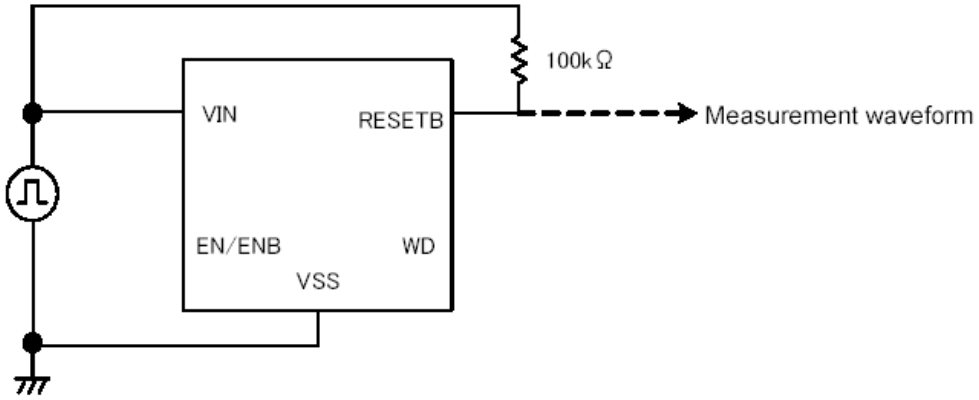


Circuit ③

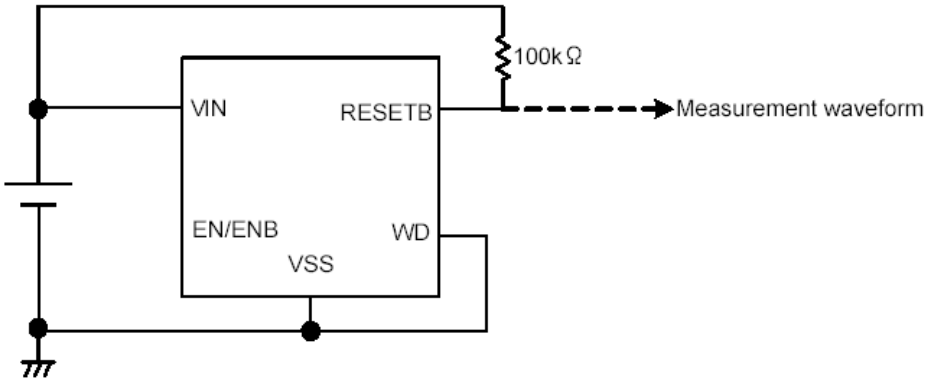


■TEST CIRCUITS (Continued)

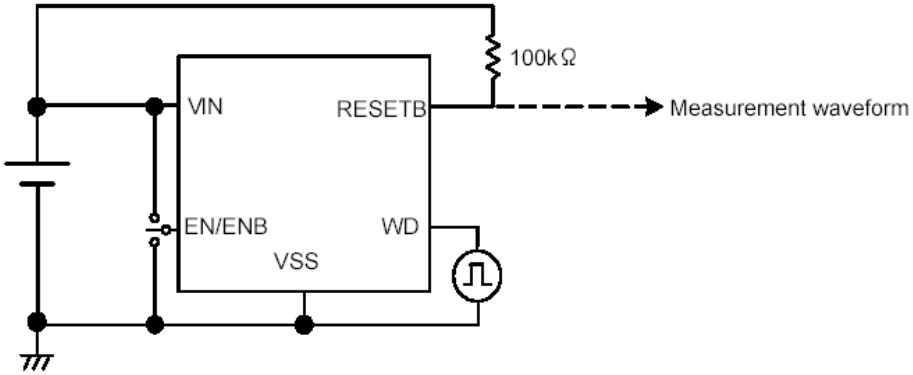
Circuit ④

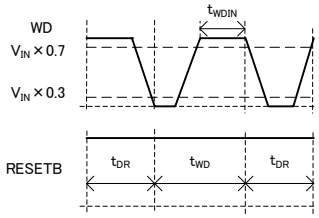


Circuit ⑤



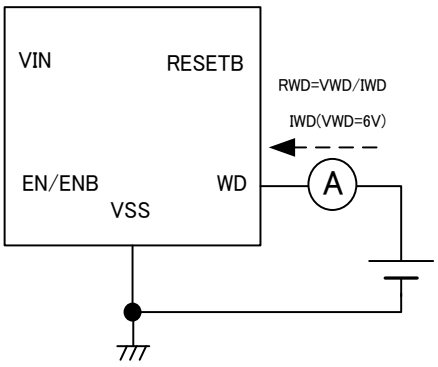
Circuit ⑥



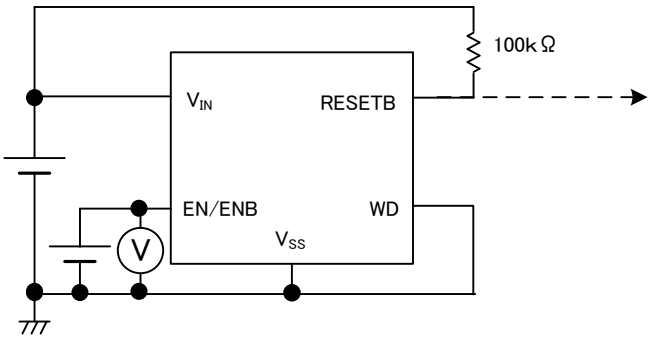


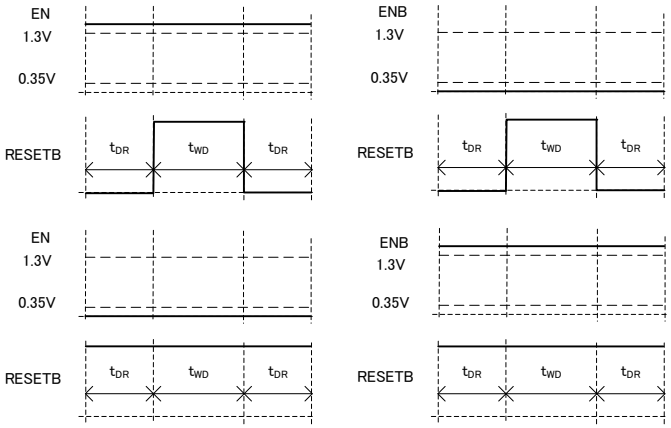
■TEST CIRCUITS (Continued)

Circuit ⑦



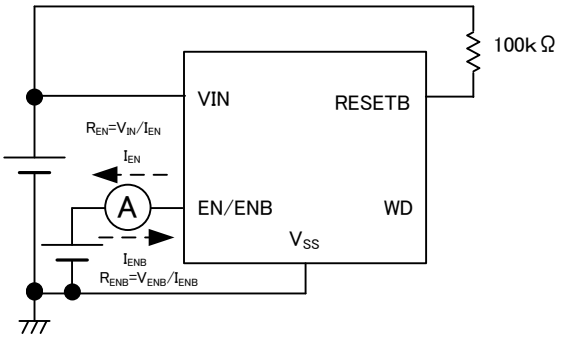
Circuit ⑧





Note: The above reference is about the EN/ENB logic operation.

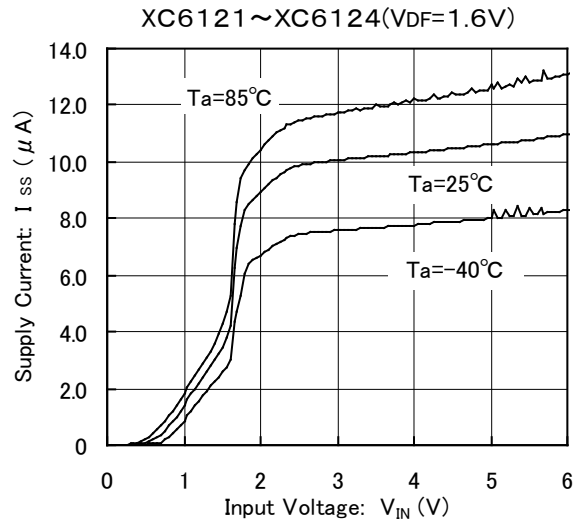
Circuit ⑨

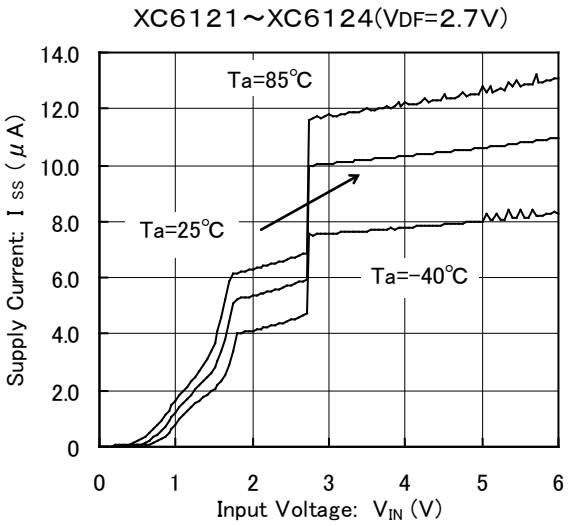


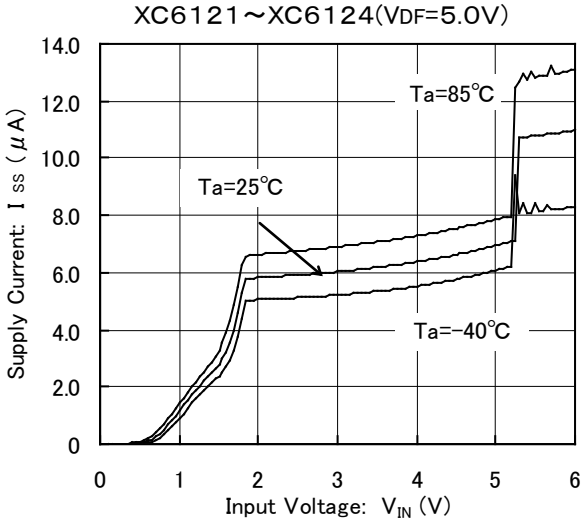
Note:
XC6122 series has EN pin,
XC6124 Series has ENB pin.

■TYPICAL PERFORMANCE CHARACTERISTICS

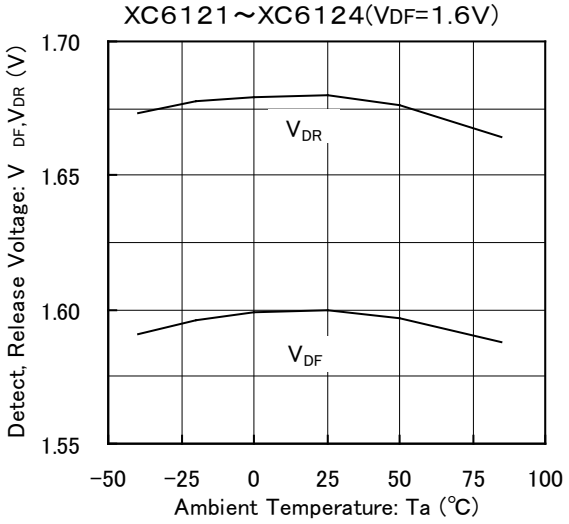
(1) Supply Current vs. Input Voltage

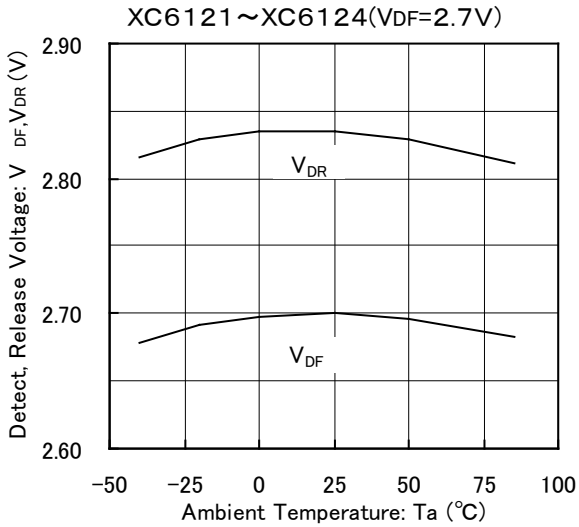






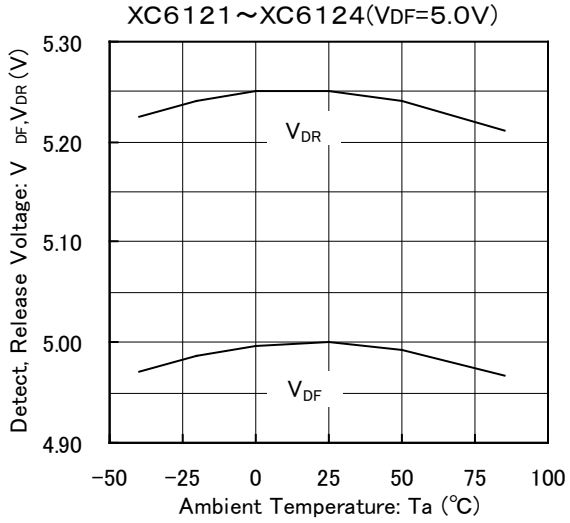
(2) Detect, Release Voltage vs. Ambient Temperature



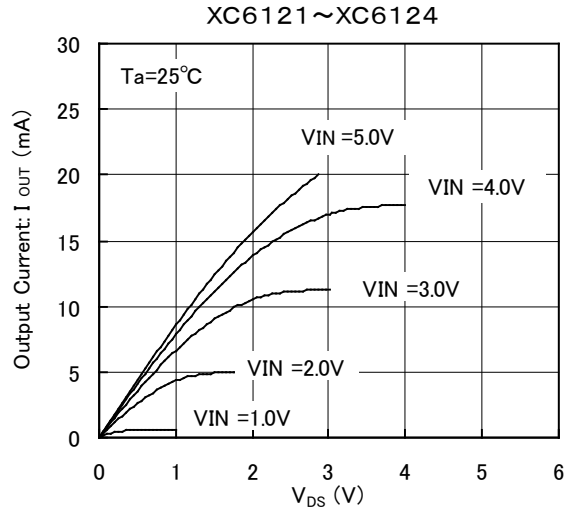


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

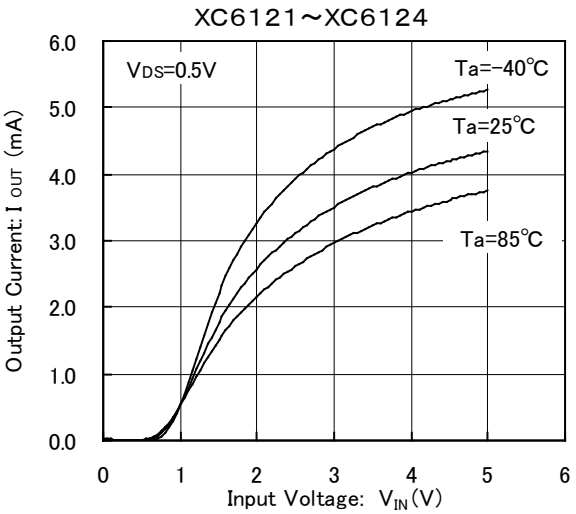
(2) Detect, Release Voltage vs. Ambient Temperature (Continued)



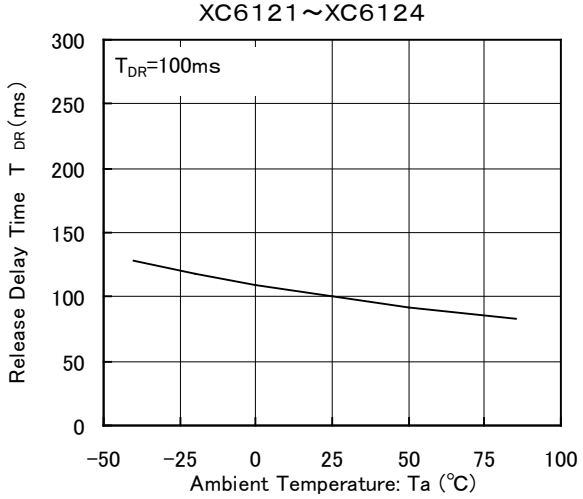
(3) Nch Driver Output Current vs. VDS

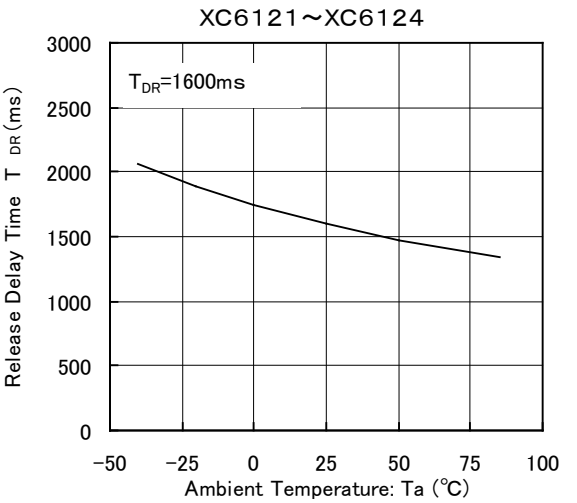


(4) Driver Output Current vs. Input Voltage



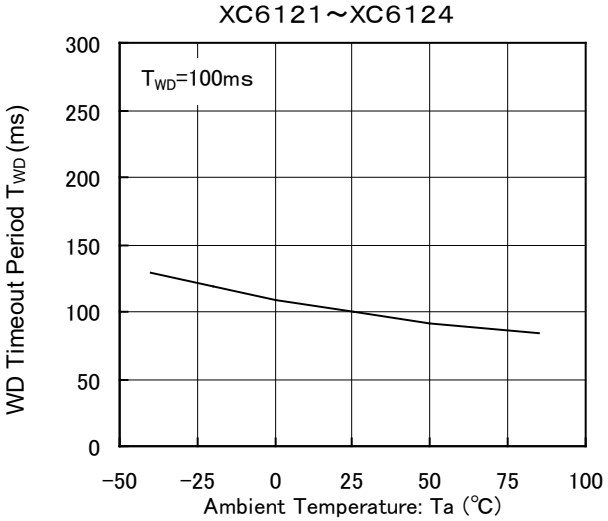
(5) Release Delay Time vs. Ambient Temperature

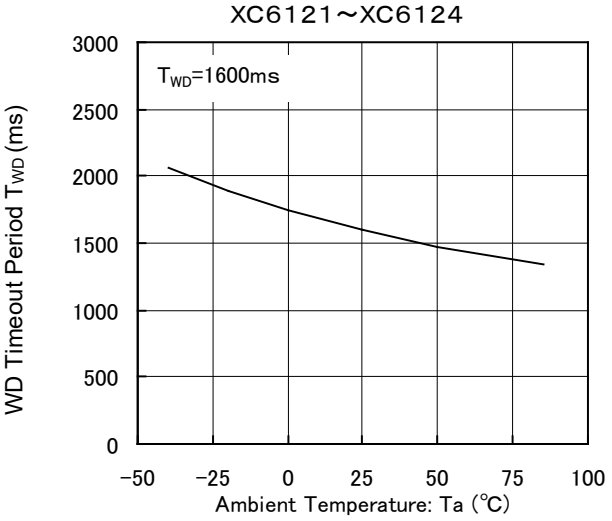




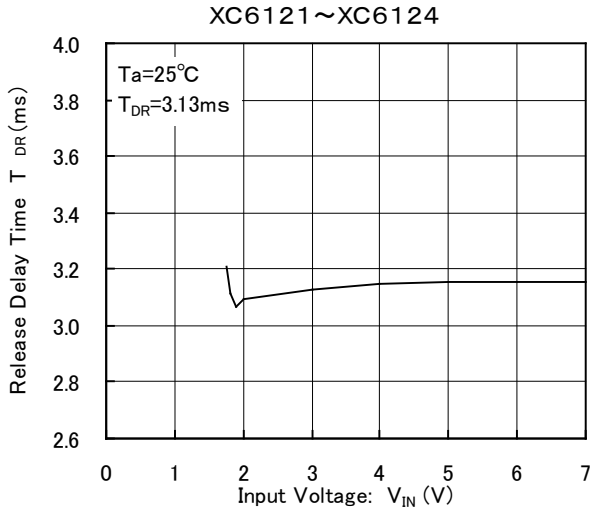
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(6) Watchdog Timeout Period vs. Ambient Temperature

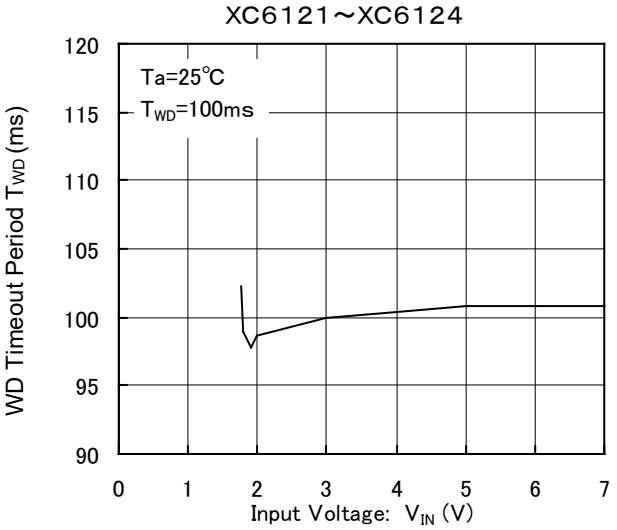




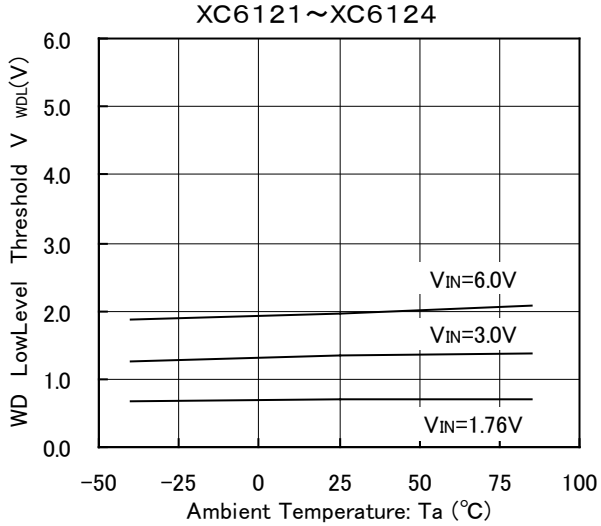
(7) Release Delay Time vs. Input Voltage



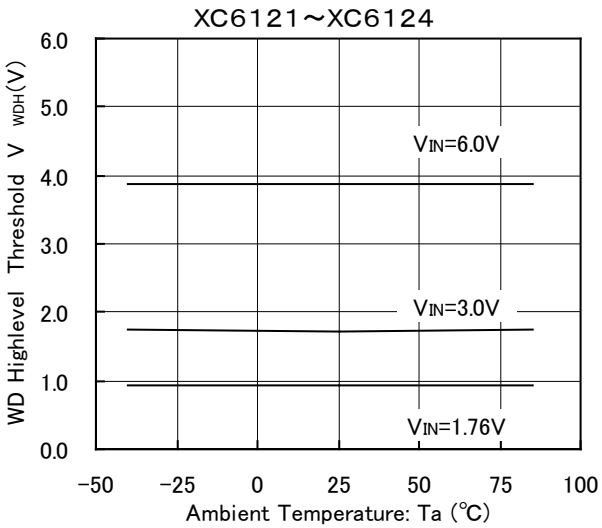
(8) Watchdog Timeout Period vs. Input Voltage



(9) Watchdog Low Level Threshold vs. Ambient Temperature

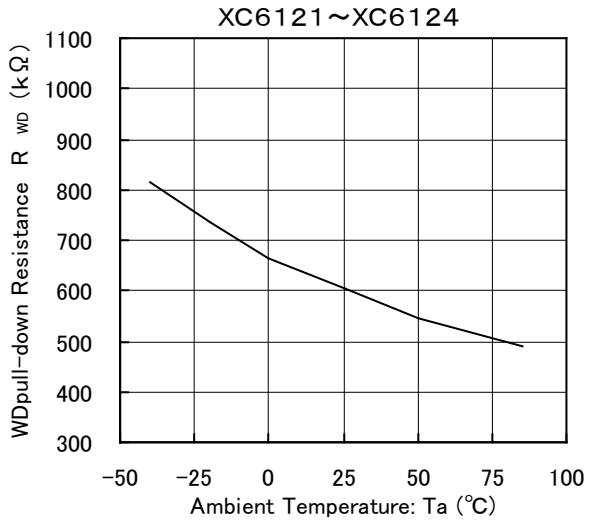


(10) Watchdog High Level Threshold vs. Ambient Temperature

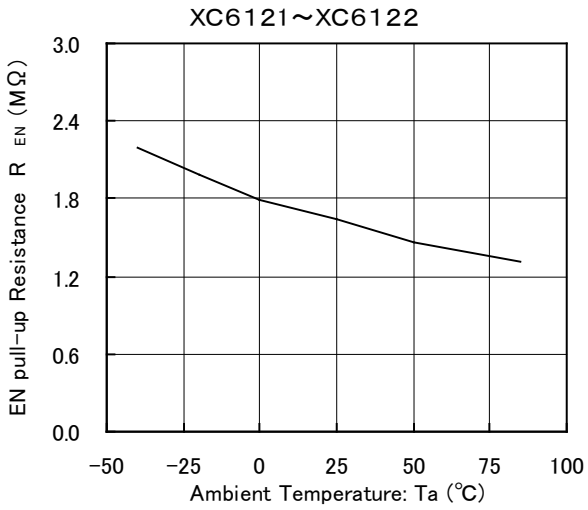


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

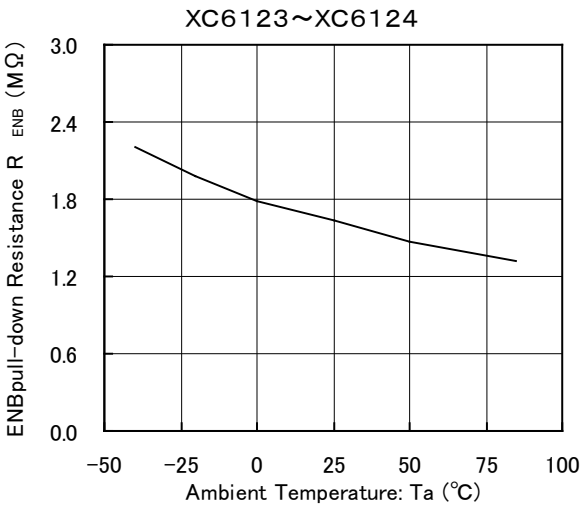
(11) Watchdog Pull-Down Resistance vs. Ambient Temperature



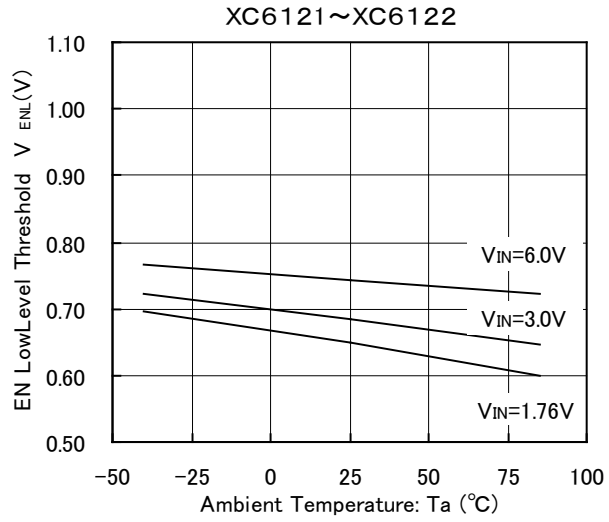
(12) EN Pull-Up Resistance vs. Ambient Temperature



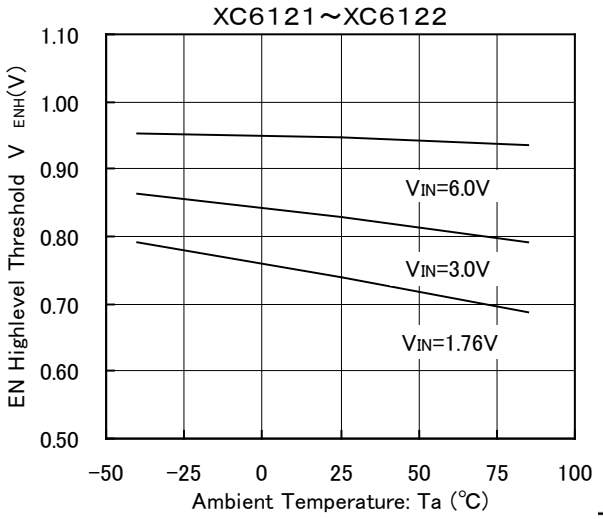
(13) ENB Pull-Down Resistance vs. Ambient Temperature



(14) EN Ligh Level Voltage vs. Ambient Temperature

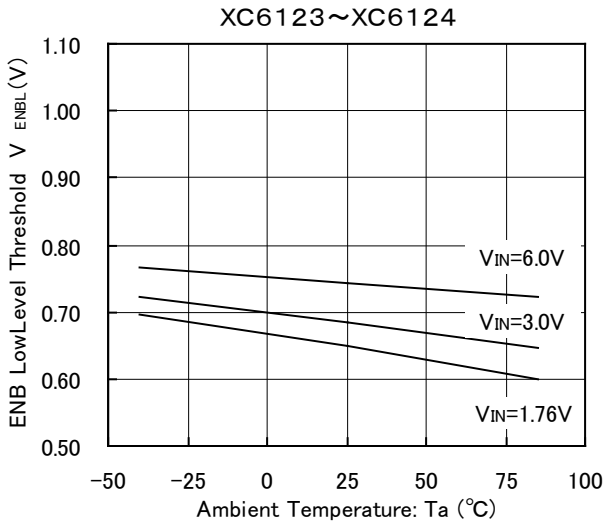


(15) EN High Level Voltage vs. Ambient Temperature

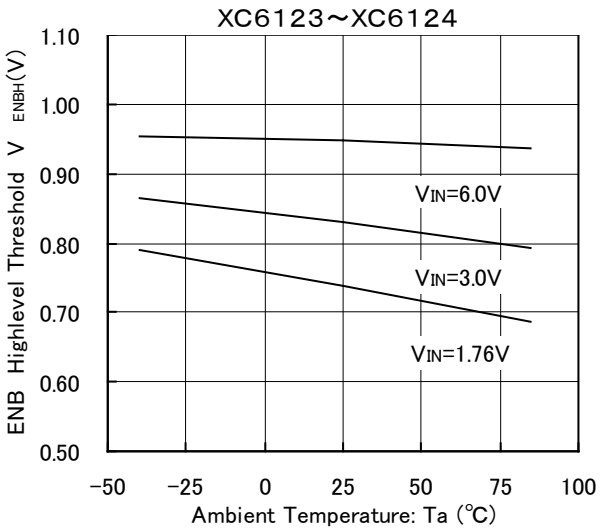


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(16) ENB Low Level Voltage vs. Ambient Temperature



(17) ENB High Level Voltage vs. Ambient Temperature



■PACKAGING INFORMATION

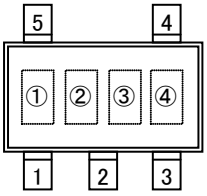
For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
SOT-26	SOT-26 PKG	SOT-26 Power Dissipation
USP-6C	USP-6C PKG	USP-6C Power Dissipation

■MARKING RULE

① represents product series

MARK	PRODUCT SERIES
E	XC6121******
F	XC6122******
H	XC6123******
K	XC6124******



SOT-25

② represents release delay time and watchdog timeout period

XC6121 Series

MARK	RELEASE DELAY TIME	WATCH DOG TIMEOUT PERIOD	PRODUCT SERIES
0	3.13ms	50ms	XC6121A2****
1	3.13 ms	100ms	XC6121A3****
2	3.13 ms	200ms	XC6121A4****
3	3.13 ms	400ms	XC6121A5****
4	3.13 ms	800ms	XC6121A7****
5	3.13 ms	1.6s	XC6121A6****
6	50ms	50ms	XC6121C2****
7	50ms	100ms	XC6121C3****
8	50ms	200ms	XC6121C4****
9	50ms	400ms	XC6121C5****
A	50ms	800ms	XC6121C7****
B	50ms	1.6s	XC6121C6****
H	100ms	100ms	XC6121D3****
C	100ms	200ms	XC6121D4****
L	100ms	400ms	XC6121D5****
D	100ms	800ms	XC6121D7****
M	100ms	1.6s	XC6121D6****
E	200ms	200ms	XC6121E4****
R	200ms	400ms	XC6121E5****
F	200ms	800ms	XC6121E7****
S	200ms	1.6s	XC6121E6****
T	400ms	400ms	XC6121F5****
K	400ms	800ms	XC6121F7****
U	400ms	1.6s	XC6121F6****

XC6122/XC6123/XC6124 Series

MARK	RELEASE DELAY TIME	WATCH DOG TIMEOUT PERIOD	PRODUCT SERIES
N	3.13ms	50ms	XC612*A2****
P	3.13ms	100ms	XC612*A3****
R	3.13ms	200ms	XC612*A4****
S	3.13ms	400ms	XC612*A5****
T	3.13ms	800ms	XC612*A7****
U	3.13ms	1.6s	XC612*A6****
V	50ms	50ms	XC612*C2****
X	50ms	100ms	XC612*C3****
Y	50ms	200ms	XC612*C4****
Z	50ms	400ms	XC612*C5****
A	50ms	800ms	XC612*C7****
B	50ms	1.6s	XC612*C6****
A	100ms	100ms	XC612*D3****
C	100ms	200ms	XC612*D4****
B	100ms	400ms	XC612*D5****
D	100ms	800ms	XC612*D7****
C	100ms	1.6s	XC612*D6****
D	200ms	200ms	XC612*E4****
E	200ms	400ms	XC612*E5****
H	200ms	800ms	XC612*E7****
F	200ms	1.6s	XC612*E6****
K	400ms	400ms	XC612*F5****
M	400ms	800ms	XC612*F7****
L	400ms	1.6s	XC612*F6****

■MARKING RULE (Continued)

③ represents detect voltage

XC6121 Series

MARK	DETECT VOLTAGE (V)	PRODUCT SERIES
F	1.6	XC6121**16**
H	1.7	XC6121**17**
K	1.8	XC6121**18**
L	1.9	XC6121**19**
M	2.0	XC6121**20**
N	2.1	XC6121**21**
P	2.2	XC6121**22**
R	2.3	XC6121**23**
S	2.4	XC6121**24**
T	2.5	XC6121**25**
U	2.6	XC6121**26**
V	2.7	XC6121**27**
X	2.8	XC6121**28**
Y	2.9	XC6121**29**
Z	3.0	XC6121**30**
0	3.1	XC6121**31**
1	3.2	XC6121**32**
2	3.3	XC6121**33**
3	3.4	XC6121**34**
4	3.5	XC6121**35**
5	3.6	XC6121**36**
6	3.7	XC6121**37**
7	3.8	XC6121**38**
8	3.9	XC6121**39**
9	4.0	XC6121**40**
A	41	XC6121**41**
B	4.2	XC6121**42**
C	4.3	XC6121**43**
D	4.4	XC6121**44**
E	4.5	XC6121**45**
F	4.6	XC6121**46**
H	4.7	XC6121**47**
K	4.8	XC6121**48**
L	4.9	XC6121**49**
M	5.0	XC6121**50**

XC6122/XC6123/XC6124 Series

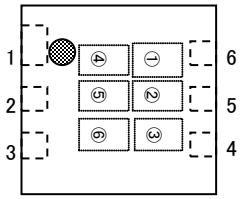
MARK	DETECT VOLTAGE (V)	PRODUCT SERIES
H	1.6	XC612***16**
K	1.7	XC612***17**
L	1.8	XC612***18**
M	1.9	XC612***19**
N	2.0	XC612***20**
P	2.1	XC612***21**
R	2.2	XC612***22**
S	2.3	XC612***23**
T	2.4	XC612***24**
U	2.5	XC612***25**
V	2.6	XC612***26**
X	2.7	XC612***27**
Y	2.8	XC612***28**
Z	2.9	XC612***29**
0	3.0	XC612***30**
1	3.1	XC612***31**
2	3.2	XC612***32**
3	3.3	XC612***33**
4	3.4	XC612***34**
5	3.5	XC612***35**
6	3.6	XC612***36**
7	3.7	XC612***37**
8	3.8	XC612***38**
9	3.9	XC612***39**
A	4.0	XC612***40**
B	41	XC612***41**
C	4.2	XC612***42**
D	4.3	XC612***43**
E	4.4	XC612***44**
F	4.5	XC612***45**
H	4.6	XC612***46**
K	4.7	XC612***47**
L	4.8	XC612***48**
M	4.9	XC612***49**
N	5.0	XC612***50**

④ represents production lot number
0 to 9 and A to Z and inverted 0 to 9 and A to Z repeated. (G, I, J, O, Q, W excluded.)

■MARKING RULE (Continued)

① represents product series

MARK	PRODUCT SERIES
P	XC6121******
K	XC6122******
R	XC6123******
U	XC6124******



USP-6C

② represents release delay time

MARK	RELEASE DELAY TIME	PRODUCT SERIES
A	3.13ms	XC612*A*****
C	50ms	XC612*C*****
D	100ms	XC612*D*****
E	200ms	XC612*E*****
F	400ms	XC612*F*****

③ represents watchdog timeout period

MARK	WATCHDOG TIMEOUT PERIOD	PRODUCT SERIES
2	50ms	XC612*2*****
3	100ms	XC612*3*****
4	200ms	XC612*4*****
5	400ms	XC612*5*****
7	800ms	XC612*7*****
6	1.6s	XC612*6*****

④⑤ represents detect voltage

MARK		DETECT VOLTAGE (V)	PRODUCT SERIES
④	⑤		
3	3	3.3	XC612***33**
5	0	5.0	XC612***50**

⑥ represents production lot number
0 to 9 and A to Z repeated. (G, I, J, O, Q, W excluded.)
*No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

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