

XD9707/XD9708 Series

ETR05083-002a

Qualified for automotive applications up to 125°C Ta,
36V & 600mA Synchronous Step-Down DC/DC Converters

☆AEC-Q100 Grade1

■ GENERAL DESCRIPTION

The XD9707/XD9708 series are 36V operation synchronous step-down DC/DC converter ICs with a built-in P-channel MOS driver FET and N-channel MOS switching FET. The XD9707/XD9708 series has an operating voltage range of 3V to 36V, a switching frequency of 2.2MHz, and the circuit scheme of synchronous rectification to be a highly efficient and stable power supply. An internal reference voltage source of 0.75V is available, and the output voltage can be set to 1.8V to 12V by external resistors (R_{FB1} and R_{FB2}).

The soft-start time is internally set to 2.0ms (TYP.), but can be adjusted to set a longer time using an external resistor and capacitor. With the built-in UVLO function, the driver FET is forced OFF when input voltage becomes 2.7V or lower.

The output state can be monitored using the power good function.

Over-current protection and thermal shutdown are built in as protection function, and it can be used safely even in the case of short circuit. Internal protection circuits include over current protection and thermal shutdown circuits to enable safe use.

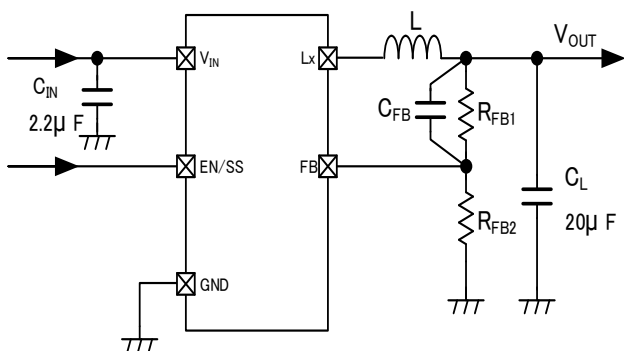
■ APPLICATIONS

- Automotive Body Control
- Automotive Infotainment
- Automotive accessories
 - Drive recorder
 - Car-mounted camera
 - ETC
- Industrial Equipment

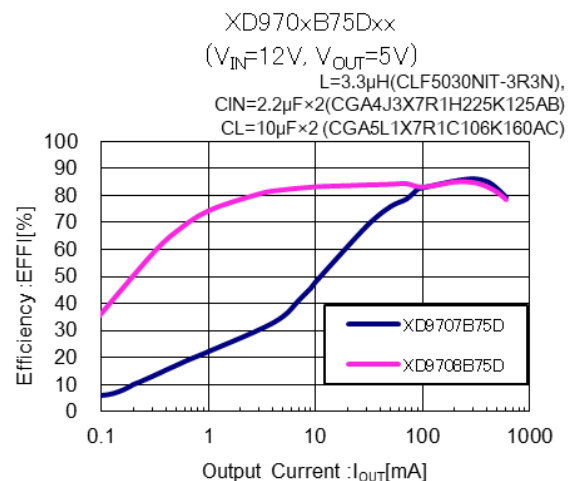
■ FEATURES

- Input Voltage Range : 3.0V ~ 36.0V (Absolute Max 40V)
- Output Voltage Range : 1.8V ~ 12.0V
- FB Voltage : 0.75V ± 1.5%
- Oscillation Frequency : 2.2MHz
- Output Current : 600mA
- Quiescent Current : 13.5µA (XD9708)
- Control Methods : PWM control (XD9707)
: PWM/PFM Auto (XD9708)
: Efficiency 85%@12V→5V,300mA
- Soft-start Time : Adjustable by RC
- Protection functions : Over Current Protection (Automatic Recovery)
: Thermal Shutdown
- Output Capacitor : Ceramic Capacitor
- Operating Ambient Temperature : -40°C ~ 105°C
- Packages : SOT-89-5
: USP-6C
- Environmentally Friendly : EU RoHS Compliant, Pb Free

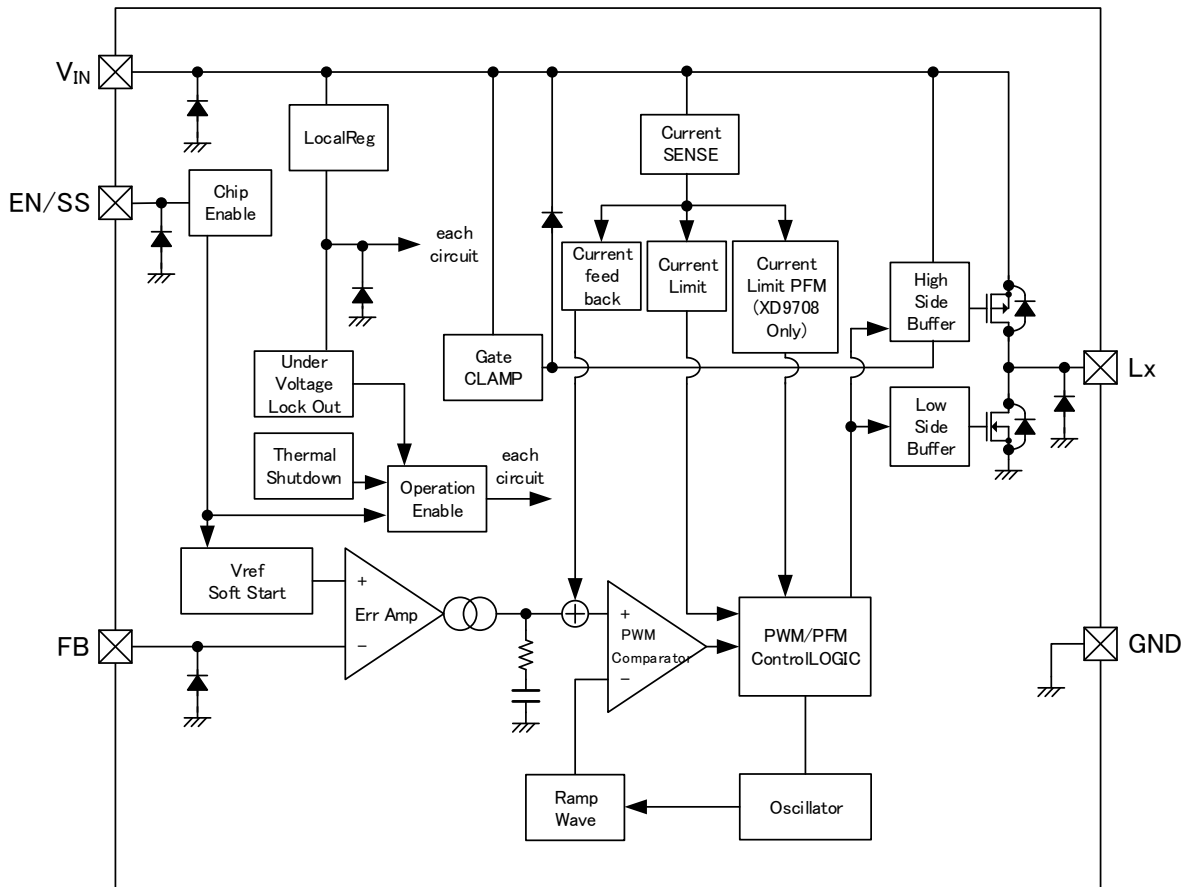
■ TYPICAL APPLICATION CIRCUIT



■ TYPICAL PERFORMANCE CHARACTERISTICS



■ BLOCK DIAGRAM



* Diodes inside the circuit are ESD protection diodes and parasitic diodes.

■ PRODUCT CLASSIFICATION

● Ordering Information

XD9707①②③④⑤⑥-⑦^(*) PWM control

XD9708①②③④⑤⑥-⑦^(*) PWM/PFM Auto

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	B	Refer to Selection Guide
②③	FB Voltage	75	Output voltage can be adjusted in 1.8V to 12.0V
④	Oscillation Frequency	D	2.2MHz
⑤⑥-⑦	Packages	PR-Q ^(*)	SOT-89-5 (1,000pcs/Reel) ^(*)
		ER-Q ^(*)	USP-6C (3,000pcs/Reel) ^(*)

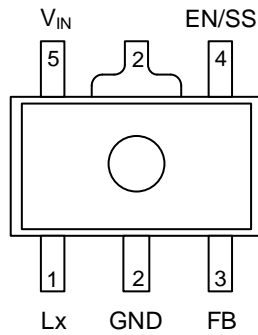
^(*) The “-Q” suffix denotes “AEC-Q100” compliant.

^(*) “Halogen and Antimony free” as well as being fully EU RoHS compliant.

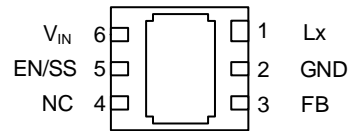
● Selection Guide

FUNCTION	B TYPE
Chip Enable	Yes
UVLO	Yes
Thermal Shutdown	Yes
Soft Start	Yes
Current Limiter (Automatic Recovery)	Yes

PIN CONFIGURATION



SOT-89-5
(TOP VIEW)



USP-6C
(BOTTOM VIEW)

* The dissipation pad for the USP-6C package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the GND (No. 2) pin.

PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-89-5	USP-6C		
1	1	Lx	Switching Output
2	2	GND	Ground
3	3	FB	Output Voltage Sense
-	4	NC	No Connection
4	5	EN/SS	Enable Soft-start
5	6	V _{IN}	Power Input

FUNCTION CHART

PIN NAME	SIGNAL	STATUS
EN/SS	L	Stand-by
	H	Active
	OPEN	Undefined State ^(*)

^(*) Please do not leave the EN/SS pin open. Each should have a certain voltage

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
V _{IN} Pin Voltage		V _{IN}	-0.3 ~ 40	V
EN/SS Pin Voltage		V _{EN/SS}	-0.3 ~ 40	V
FB Pin Voltage		V _{FB}	-0.3 ~ 6.2	V
Lx Pin Voltage		V _{Lx}	-0.3 ~ V _{IN} + 0.3 or 40 ^(*)	V
Lx Pin Current		I _{Lx}	1800	mA
Power Dissipation (Ta=25°C)	SOT-89-5	Pd	2150 (JESD51-7 基板) ^(*)	mW
	USP-6C		1550 (JESD51-7 基板) ^(*)	
Surge Voltage		V _{SURGE}	+46 ^(*)	V
Junction Temperature		T _j	-40 ~ 150	°C
Storage Temperature		T _{stg}	-55 ~ 150	°C

* All voltages are described based on the GND pin.

(*) The maximum value should be either V_{IN}+0.3V or 40V in the lowest.

(*) Applied Time ≤ 400ms

(*) The power dissipation figure shown is PCB mounted and is for reference only.

Please refer to PACKAGING INFORMATION for the mounting condition.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Setting Output Voltage Range	V _{OUTSET}	1.8	-	12.0	V
Input Voltage	V _{IN}	3.0	-	36.0	V
Output Current	I _{OUT}	0.0	-	600	mA
EN/SS Pin Voltage	V _{EN/SS}	0.0	-	36.0	V
Operating Ambient Temperature	T _{opr}	-40	-	125	°C

* All voltages are described based on the GND pin.

ELECTRICAL CHARACTERISTICS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT	
FB Voltage	V _{FBE}	V _{FB} =0.731V→0.769V, V _{FB} Voltage when Lx pin voltage changes from "H" level to "L" level	0.739	0.750	0.761	V	②	
		-40°C ≤ Ta ≤ 125°C	0.728	-	0.773			
Setting Output Voltage Range ^(*)	V _{OUTSET}	-	1.8	-	12.0	V	-	
Operating Input Voltage Range ^(*)	V _{IN}	-	3.0	-	36.0	V	-	
UVLO Detect Voltage	V _{UVLOD}	V _{EN/SS} =12V, V _{IN} :2.87V→2.53V, V _{FB} =0V V _{IN} Voltage which Lx pin voltage holding "H" level	2.60	2.70	2.80	V	②	
		-40°C ≤ Ta ≤ 125°C	2.50	-	2.87			
UVLO Release Voltage	V _{UVLOR}	V _{EN/SS} =12V, V _{IN} :2.63V→2.97V, V _{FB} =0V V _{IN} Voltage which Lx pin voltage holding "L" level	2.70	2.80	2.90	V	②	
		-40°C ≤ Ta ≤ 125°C	2.60	-	2.97			
Quiescent Current	I _q	V _{FB} =0.825V	XD9707	-	290	500	μA	④
				-40°C ≤ Ta ≤ 125°C	-	-		
			XD9708	-	13.5	22.0		
				-40°C ≤ Ta ≤ 125°C	-	-		
Stand-by Current	I _{STBY}	V _{IN} =12V, V _{EN/SS} =V _{FB} =0V	-	1.65	2.50	μA	④	
			-40°C ≤ Ta ≤ 125°C	-	-			5.85
Oscillation Frequency	f _{osc}	Connected to external components, I _{OUT} =200mA	2.013	2.200	2.387	MHz	①	
			-40°C ≤ Ta ≤ 125°C	1.936	-			2.464
Minimum On Time	t _{ONMIN}	Connected to external components	-	85 ^(*)	-	ns	①	
Minimum Duty Cycle	D _{MIN}	V _{FB} =0.825V	-40°C ≤ Ta ≤ 125°C	-	-	0	%	②
Maximum Duty Cycle	D _{MAX}	V _{FB} =0.675V	-40°C ≤ Ta ≤ 125°C	100	-	-	%	②
Lx SW "H" On Resistance	R _{LxH}	V _{FB} =0.675V, I _{Lx} =200mA	-	1.20	1.38	Ω	⑤	
Lx SW "L" On Resistance	R _{LxL}	-	-	0.60 ^(*)	-	Ω	⑤	
High side Current Limit ^(*)	I _{LIMH}	V _{FB} =V _{FBE} ×0.98	1.00	1.30	-	A	⑤	
Internal Soft-Start Time	t _{SS1}	V _{FB} =0.675V	1.0	2.0	4.0	ms	②	
External Soft-Start Time	t _{SS2}	V _{FB} =0.675V R _{SS} =430KΩ, C _{SS} =0.47μF	21	26	33	ms	③	

Test Condition: Unless otherwise stated, V_{IN}=12V, V_{EN/SS}=12V

The ambient temperature range (-40°C ≤ Ta ≤ 105°C) is design Value.

Peripheral parts connection conditions : L=3.3μH, R_{FB1}=43kΩ, R_{FB2}=7.5kΩ, C_{FB}=180pF, C_L=10μF×2, C_{IN}=2.2μF

^(*) Design reference value. This parameter is provided only for reference.

^(*) Current limit denotes the level of detection at peak of coil current.

■ ELECTRICAL CHARACTERISTICS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
PFM Switch Current	IPFM	Connected to external components, VIN=VEN/SS=12V, IOUT=1mA	-	400	-	mA	①
Efficiency	EFFI	Connected to external components, VIN=12V, VOUT=5V, IOUT=300mA	-	85	-	%	①
FB Voltage Temperature Characteristics	$\frac{\Delta V_{FB}}{(\Delta T_{opr} \cdot V_{FBE})}$	-40°C ≤ T _{opr} ≤ 125°C	-	±100	-	ppm/°C	①
FB "H" Current	IFBH	VIN=VEN/SS=36V, VFB=3.0V -40°C ≤ Ta ≤ 125°C	-0.1	0.0	0.1	μA	①
FB "L" Current	IFBL	VIN=VEN/SS=36V, VFB=0V -40°C ≤ Ta ≤ 125°C	-0.1	0.0	0.1	μA	④
EN/SS "H" Voltage	VEN/SSH	VEN/SS=0.3V→2.5V, VFB=0.71V VEN/SS Voltage when Lx pin voltage changes from "L" level to "H" level 40°C ≤ Ta ≤ 125°C	2.5	-	36	V	①
EN/SS "L" Voltage	VEN/SSL	VEN/SS=2.5V→0.3V, VFB=0.71V VEN/SS Voltage when Lx pin voltage changes from "H" level to "L" level -40°C ≤ Ta ≤ 125°C	GND	-	0.3	V	①
EN/SS "H" Current	IEN/SSH	VIN=VEN/SS=36V, VFB=0.825V -40°C ≤ Ta ≤ 125°C	-	0.1	0.3	μA	④
EN/SS "L" Current	IEN/SSL	VIN=36V, VEN/SS=0V, VFB=0.825V -40°C ≤ Ta ≤ 125°C	-0.1	0.0	0.1	μA	①
Thermal Shutdown Temperature	T _{TSD}	Junction Temperature	-	165	-	°C	-
Hysteresis Width	T _{HYS}	Junction Temperature	-	25	-	°C	-

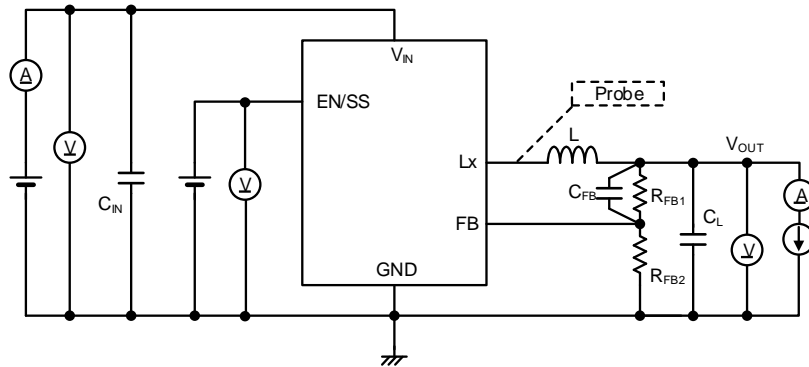
Test Condition: Unless otherwise stated, VIN=12V, VEN/SS=12V

The ambient temperature range (-40°C ≤ Ta ≤ 105°C) is design Value.

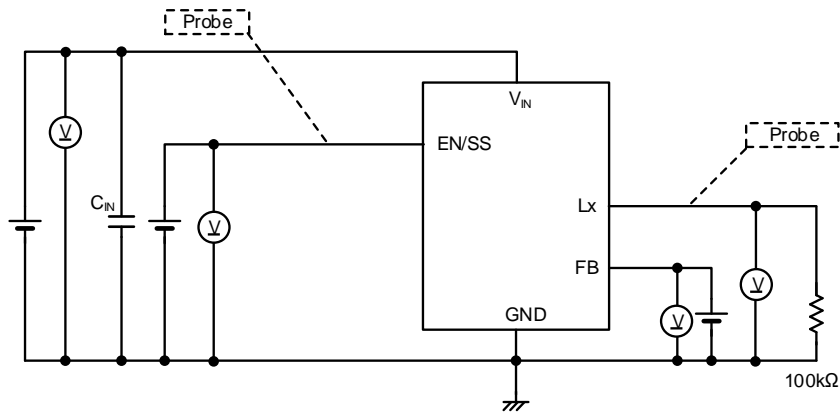
Peripheral parts connection conditions : L=3.3μH, RFB1=43kΩ, RFB2=7.5kΩ, CFB=180pF, CL=10μF×2, CIN=2.2μF

TEST CIRCUITS

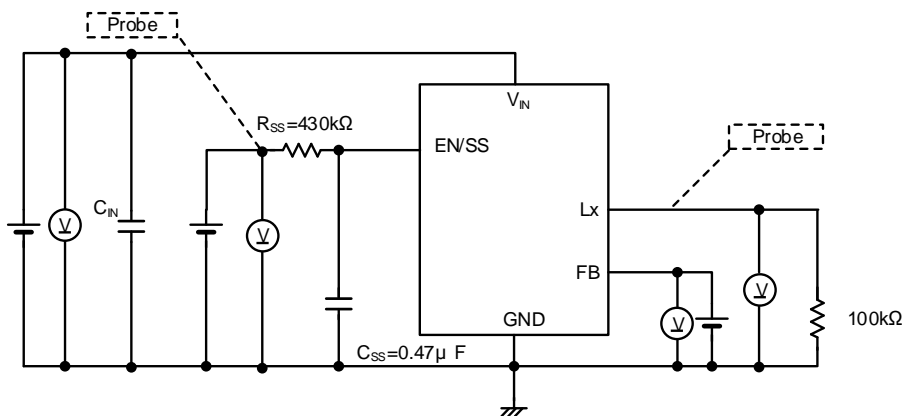
CIRCUIT①



CIRCUIT②

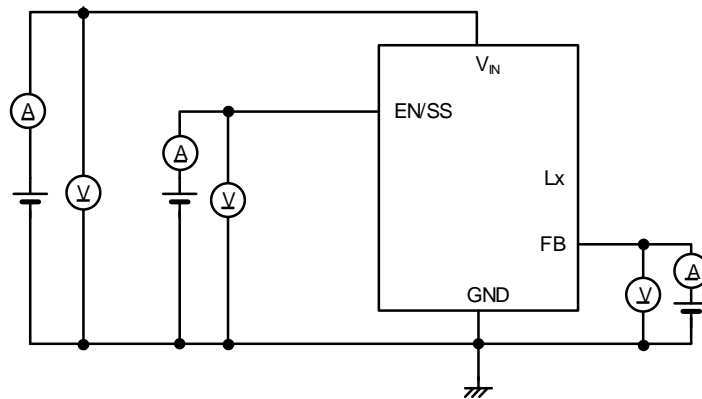


CIRCUIT③

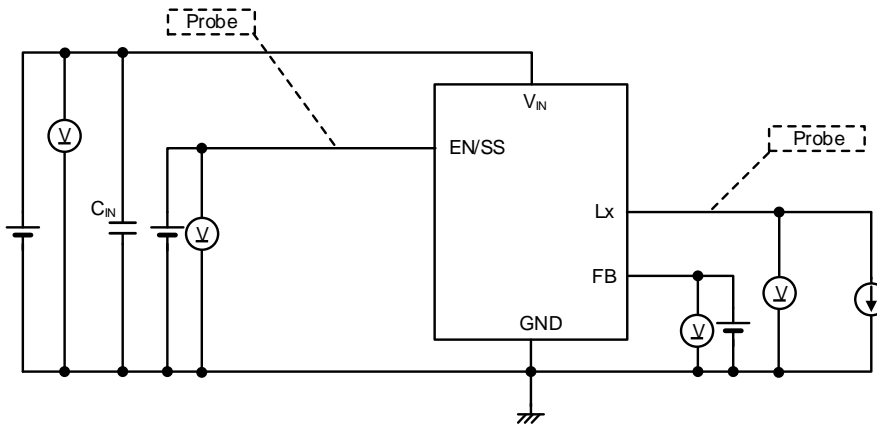


■ TEST CIRCUITS

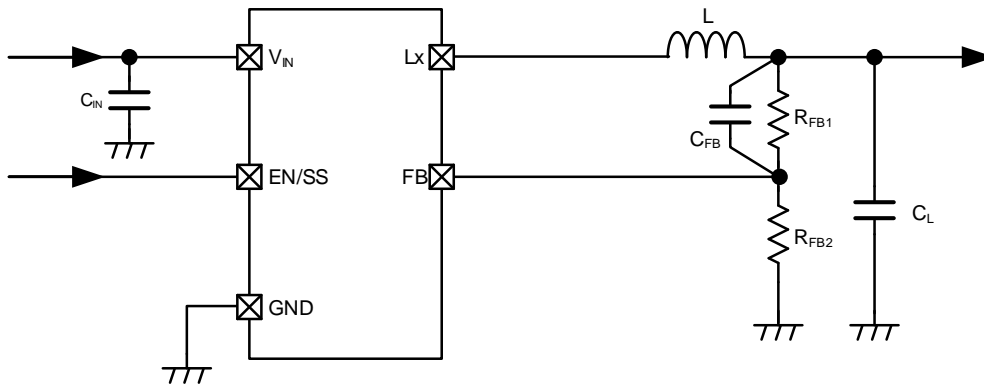
CIRCUIT④



CIRCUIT⑤



TYPICAL APPLICATION CIRCUIT / Parts Selection Method



<Inductance value setting>

For the XD9707/XD9708 Series, operation is optimized by setting the following inductance value according to the setting output voltage.

【Typical Examples】

	CONDITIONS	MANUFACTURER	PRODUCT NUMBER	VALUE
L	$1.8V < V_{OUTSET} \leq 2V$	TDK	CLF5030NIT-1R5N-D	1.5 μ H
	$2V < V_{OUTSET} \leq 3.3V$	TDK	CLF5030NIT-2R2N-D	2.2 μ H
	$3.3V < V_{OUTSET} \leq 6V$	TDK	CLF5030NIT-3R3N-D	3.3 μ H
	$6V < V_{OUTSET} \leq 12V$	TDK	CLF5030NIT-4R7N-D	4.7 μ H
C _{IN1} ^(*)	$V_{IN} < 20V$	TDK	CGA4J3X7R1H225K125AB	2.2 μ F/50V
	$V_{IN} \geq 20V$	TDK	CGA4J3X7R1H225K125AB	2.2 μ F/50V 2parallel
C _{IN2}	-	TDK	CGA3E2X7R1H104K080AA	0.1 μ F/50V
C _L ^(*)	-	TDK	CGA5L1X7R1V106K160AC	10 μ F/35V 2parallel

V_{OUTSET}: Output voltage setting

^(*) For C_{IN1}, use a capacitor with the same or higher effective capacity value as the recommended components.

^(*) For C_L, use a capacitor with the same or higher effective capacity value as the recommended components.
If a capacitor with a low effective capacity value is used, the output voltage may become unstable.
However, if large capacity capacitors, such as electrolytic capacitors, are connected in parallel, the inrush current during startup could increase or the output could become unstable.

■ TYPICAL APPLICATION CIRCUIT / Parts Selection Method (Continued)

< Output voltage setting >

The output voltage can be set by adding an external dividing resistor.
The output voltage is determined by the equation below based on the values of R_{FB1} and R_{FB2} .

$$V_{OUTSET} = 0.75V \times (R_{FB1} + R_{FB2}) / R_{FB2}$$

With $R_{FB2} \leq 7.5k\Omega$

< C_{FB} setting >

Adjust the value of the phase compensation speed-up capacitor C_{FB} using the equation below.

$$C_{FB} = \frac{1}{2\pi \times fzfb \times R_{FB1}}$$

$$fzfb = \frac{1}{2\pi \sqrt{C_L \times L}}$$

【Typical Example】

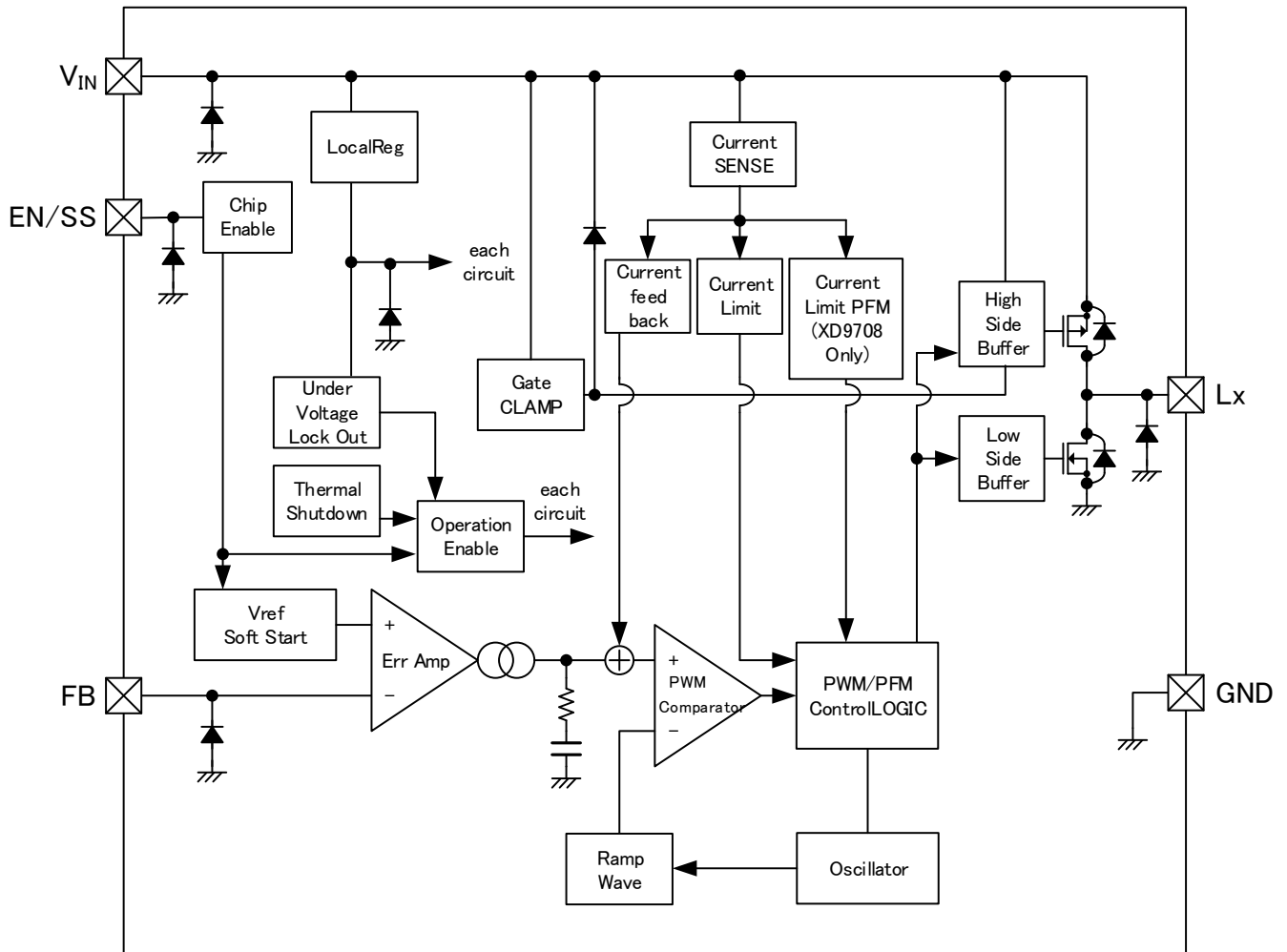
XD9707B75Dxx					
V_{OUTSET}	R_{FB1}	R_{FB2}	L	C_{FB}	fzfb
1.8V	6.8k Ω	4.7k Ω	1.5 μ H	820pF	29.1kHz
3.3V	16k Ω	4.7k Ω	2.2 μ H	470pF	24.0kHz
5.0V	43k Ω	7.5k Ω	3.3 μ H	180pF	19.6kHz
12.0V	100k Ω	6.8k Ω	4.7 μ H	100pF	16.4kHz

XD9708B75Dxx					
V_{OUTSET}	R_{FB1}	R_{FB2}	L	C_{FB}	fzfb
1.8V	6.8k Ω	4.7k Ω	1.5 μ H	820pF	29.1kHz
3.3V	16k Ω	4.7k Ω	2.2 μ H	470pF	24.0kHz
5.0V	43k Ω	7.5k Ω	3.3 μ H	180pF	19.6kHz
12.0V	100k Ω	6.8k Ω	4.7 μ H	100pF	16.4kHz

OPERATIONAL EXPLANATION

The XD9707/XD9708 series consists internally of a reference voltage supply with soft-start function, a ramp wave circuit, an error amp, a PWM comparator, a High side driver FET, a Low side driver FET, a High side buffer circuit, a Low side buffer circuit, a current sense circuit, a phase compensation (Current feedback) circuit, a current limiting circuit, an under voltage lockout (UVLO) circuit, an internal power supply (Local Reg) circuit, a gate clamp (CLAMP) circuit and other elements.

The control method is the current mode control method for handling low ESR ceramic capacitors.



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

OPERATIONAL EXPLANATION(Continued)

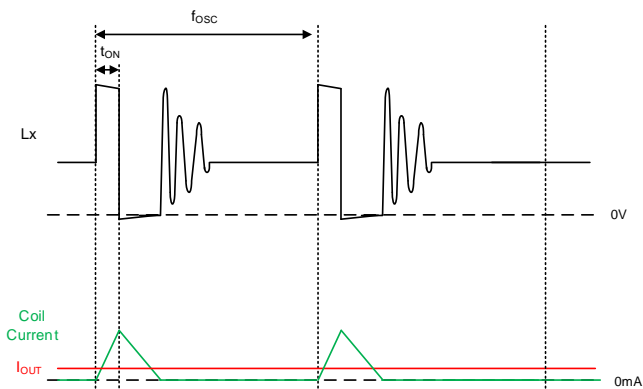
< Normal Operation >

The standard voltage V_{ref} and FB pin voltage are compared using an error amplifier and then the control signal to which phase compensation has been added to the error amplifier output is input to the PWM comparator. The PWM comparator compares the above control signal and lamp wave to control the duty width during PWM control. Continuously conducting these controls stabilizes the output voltage.

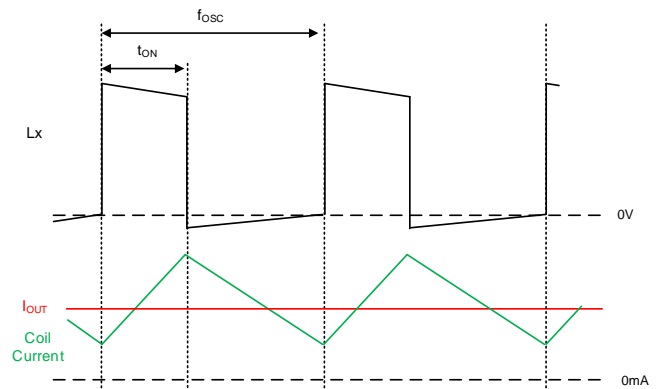
In addition, the current detecting circuit monitors the driver FET current for each switching and modulates the error amplifier output signal into a multiple feedback signal (current feedback circuit). This achieves stable feedback control even when low ESR capacitors, such as ceramic capacitors, are used to stabilize the output voltage.

XD9707 Series

The XD9707 Series (PWM control) performs switching at a set switching frequency f_{osc} regardless of the output current. At light loads the on time is short and the circuit operates in discontinuous mode, and as the output current increases, the on time becomes longer and the circuit operates in continuous mode.



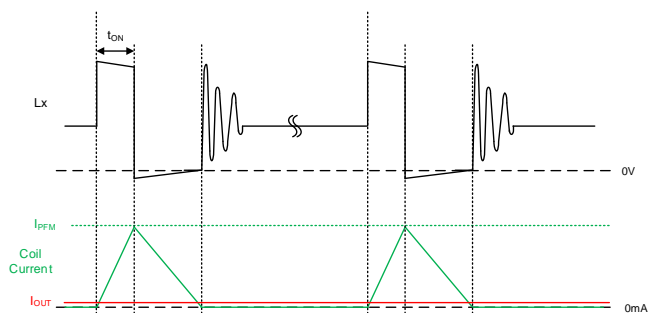
XD9707 series: Example of light load operation



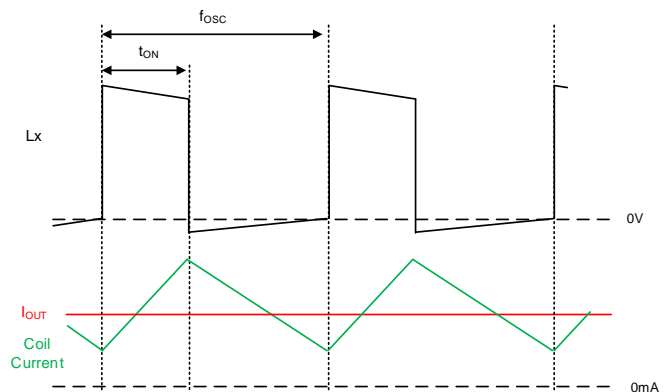
XD9707 series: Example of heavy load operation

XD9708 Series

The XD9708 Series (PWM/PFM automatic switching control) lowers the switching frequency during light loads by turning on the High side driver FET when the coil current reaches the PFM current (I_{PFM}). This operation reduces the loss during light loads and achieves high efficiency from light to heavy loads. As the output current increases, the switching frequency increases proportional to the output current, and when the switching frequency increases f_{osc} , the circuit switches from PFM control to PWM control and the switching frequency becomes fixed.



XD9708 series: Example of light load operation



XD9708 series: Example of heavy load operation

< 100% Duty Cycle Mode >

When the dropout voltage is low or there is a transient response, the circuit might change to the 100% Duty cycle mode where the High side driver FET is continuously on.

The 100% Duty cycle mode operation makes it possible to maintain the output current even when the dropout voltage is low such as when the input voltage declines due to cranking, etc.

OPERATIONAL EXPLANATION(Continued)

< CE Function >

When an "H" voltage ($V_{EN/SSH}$) is input to the EN/SS pin, normal operation is performed after the output voltage is started up by the soft start function, normal operation is performed. When the "L" voltage ($V_{EN/SSL}$) is input to the EN/SS pin, the circuit enters the standby state, the supply current is suppressed to the standby current I_{STB} (TYP. $1.65\mu A$), and the High side driver FET and Low side driver FET are turned off.

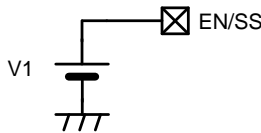
< Soft Start Function >

This function gradually starts up the output voltage to suppress the inrush current.

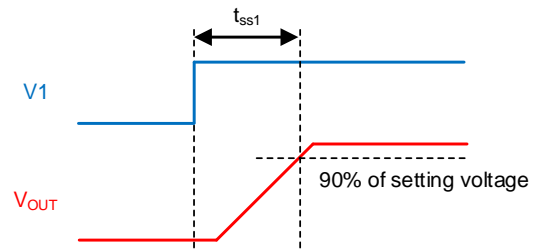
The soft start time is the time until the output voltage from $V_{EN/SSH}$ reaches 90% of the output voltage set value, and when the output voltage increases further, the soft start function is cancelled to switch to normal operation.

Internal Soft Start Time

The internal soft start time (t_{SS1}) is configured so that after the "H" voltage ($V_{EN/SSH}$) is input to the EN/SS pin, the standard voltage connected to the error amplifier increases linearly during the soft-start period. This causes the output voltage to increase proportionally to the standard voltage increase. This operation suppresses the inrush current and smoothly increases the output voltage.



< Internal soft start EN/SS circuit >



< Overview of internal soft start >

External Setting Soft Start Time

The external setting soft start time (t_{SS2}) can adjust the increase speed of the standard voltage in the IC by adjusting the EN/SS pin voltage inclination during startup using externally connected component R_{SS} and C_{SS} . This makes it possible to externally adjust the soft start time.

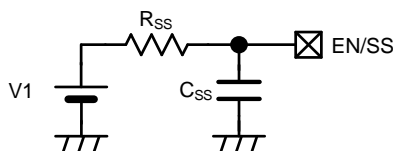
Soft start time (t_{SS2}) is approximated by the equation below according to values of $V1$, R_{SS} , and C_{SS} . When t_{SS2} is shorter than t_{SS1} , the output voltage rises at the internal soft start time.

$$t_{SS2} = C_{SS} \times R_{SS} \times \ln \left(\frac{V1}{V1 - 1.45V} \right)$$

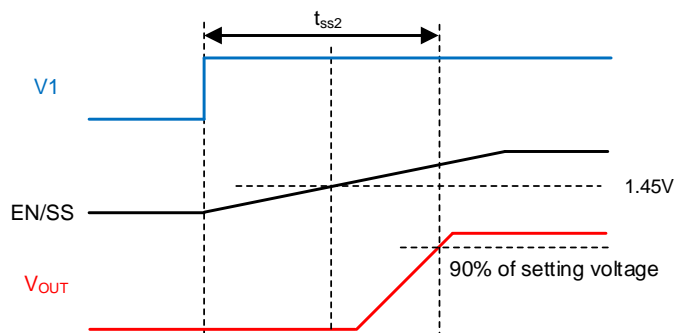
【Setting Example】

$C_{SS} = 0.47\mu F$, $R_{SS} = 430k\Omega$, $V1 = 12V$

$t_{SS2} = 0.47\mu F \times 430k\Omega \times \ln \left(\frac{12V}{12V - 1.45V} \right) = 26ms$



< External soft start EN/SS circuit >



< Overview of external soft start >

■ OPERATIONAL EXPLANATION(Continued)

< UVLO Function >

This is a function to monitor the internal power supply and to prevent the output of false pulses from the Lx pin when the output from the internal power supply is unstable at low voltages.

As the V_{IN} pin voltage goes down, the internal power supply voltage falls. So the V_{IN} voltage drops, the UVLO function is activated.

When the V_{IN} pin voltage falls below V_{UVLOD} (TYP. 2.7V), the driver transistor is forcibly turned off to prevent false pulse output due to instable operation of the internal circuits. When the V_{IN} pin voltage rises above V_{UVLOR} (TYP. 2.8V), the UVLO function is released, the soft-start function activates, and output start operation begins. Stopping by UVLO is not shutdown; only pulse output is stopped and the internal circuits continue to operate.

When the V_{IN} pin voltage falls below V_{UVLOD} (TYP. 2.7V), the UVLO function is activated.

< Thermal Shutdown Function >

A thermal shutdown (TSD) function is built in for protection from overheating. When the junction temperature reaches the thermal shutdown detection temperature T_{TSD} , the High side driver FET and Low side driver FET are compulsorily turned off.

If the driver FET continues in the off state, the junction temperature declines, and when the junction temperature falls to the thermal shutdown cancel temperature, the thermal shutdown function is cancelled and the soft-start function operates to start up the output voltage.

OPERATIONAL EXPLANATION(Continued)

< Current Limit Function >

The current limiting circuit of the XD9707/XD9708 series monitors the current that flows through the High side driver FET and Low side driver FET, and when over current is detected, the current limiting function activates.

① High side driver FET current limiting

The current in the High side driver FET is detected to equivalently monitor the peak value of the coil current. The High side driver FET current limiting function forcibly turns off the High side driver FET when the peak value of the coil current reaches the High side driver current limit value I_{LIMH} .

High side driver FET current limit value $I_{LIMH}=1.3A$ (TYP.)

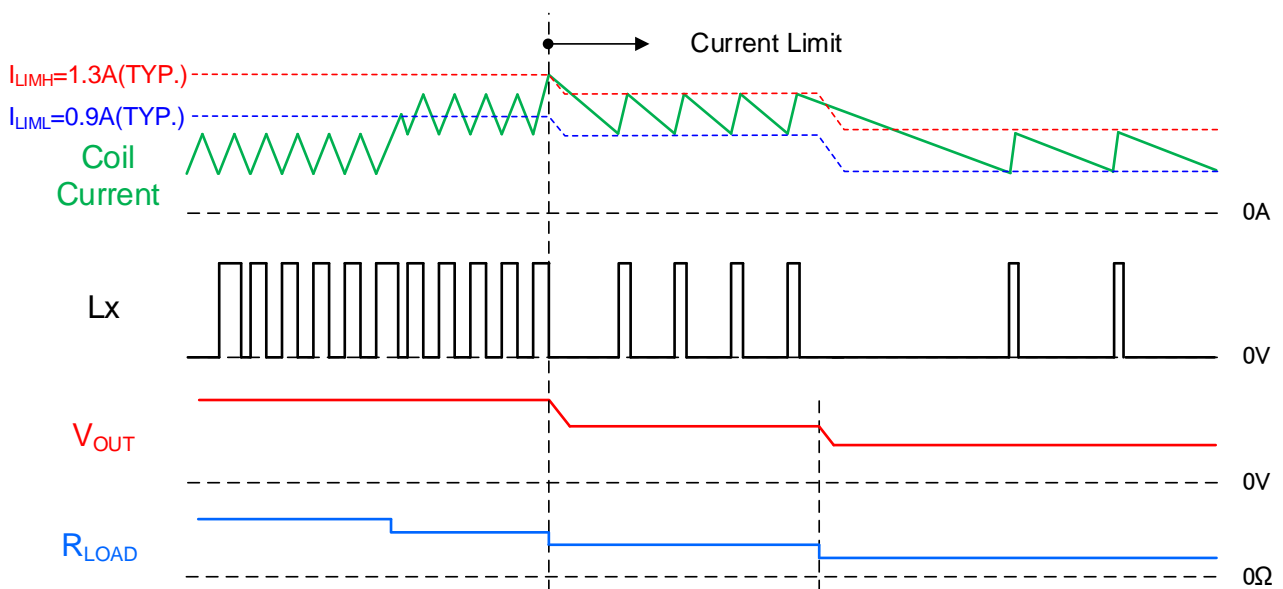
② Low side driver FET current limiting

The current in the Low side driver FET is detected to equivalently monitor the bottom value of the coil current. The Low side driver FET current limiting function operates when the High side driver FET current limiting value reaches I_{LIMH} . The Low side driver FET current limiting function prohibits the High side driver FET from turning on in an over current state where the bottom value of the coil current is higher than the Low side driver FET current limit value I_{LIML} .

Low side driver FET current limit value $I_{LIML}=0.9A$ (TYP.)

When the output current increases and reaches the current limit value, the current foldback circuit operates and lowers the output voltage and FB voltage. The I_{LIMH} and I_{LIML} decline accompanying the FB voltage decrease to restrict the output current.

When the overcurrent state is removed, the foldback circuit operation increases the I_{LIMH} and I_{LIML} together with output voltage to return the output to the output voltage set value.



■ NOTES ON USE

- 1) In the case of a temporary and transient voltage drop or voltage rise. If the absolute maximum ratings are exceeded, the IC may be deteriorate or destroyed. Also, if used under conditions outside the recommended operating range, the IC may not operate normally or may cause deterioration.

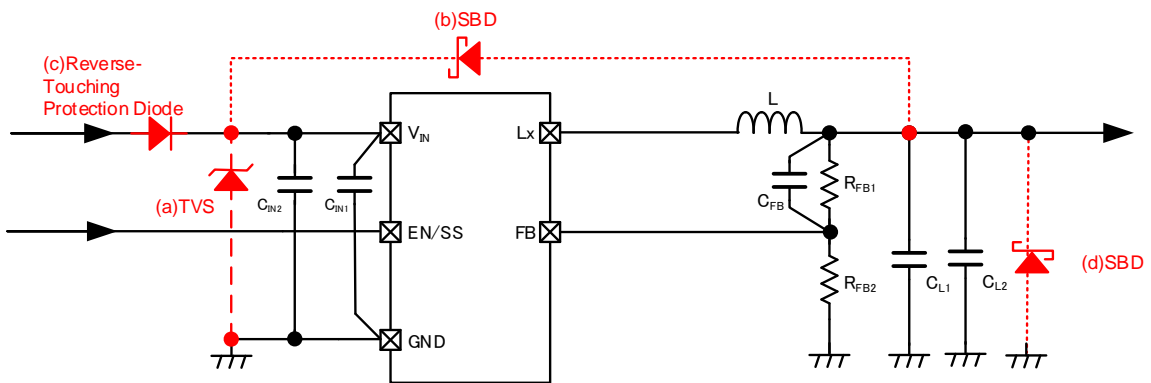
If a voltage exceeding the absolute maximum voltage is applied to the IC due to chattering caused by a mechanical switch or an external surge voltage, please use a protection element such as a TVS and a protection circuit as a countermeasure. Please see the countermeasures from (a) to (d) shown below.

(a) When voltage exceeding the absolute maximum ratings comes into the VIN pin due to the transient change on the power line, there is a possibility that the IC breaks down in the end. To prevent such a failure, please add a TVS between VIN and GND as a countermeasure

(b) When the input voltage decreases below the output voltage, there is a possibility that an overcurrent will flow in the IC's Internal parasitic diode and exceed the absolute maximum rating of the Lx pin. If the current is pulled into the input side by the low impedance between VIN -GND, then countermeasures, such as adding an SBD between VOUT-VIN, should be taken.

(c) When a negative voltage is applied to the input voltage by a reverse connection or chattering, an overcurrent could flow in the IC's parasitic diode and damage the IC. Take countermeasures, such as adding a reverse touching protection diode

(d) When a sudden surge of electrical current travels along the VOUT pin and GND due to a short-circuit, electrical resonance of a circuit involving parasitic inductor of cable related to short circuit and an output capacitor (CL) and impedance such as VOUT line generates a negative voltage exceeding the breakdown voltage and may damage the device. Take countermeasures, such as connecting a schottky diode between the VOUT and GND.



■ NOTES ON USE (Continued)

- 2) Make sure that the absolute maximum ratings of the external components and of this IC are not exceeded.
- 3) The DC/DC converter characteristics depend greatly on the externally connected components as well as on the characteristics of this IC, so refer to the specifications and standard circuit examples of each component when carefully considering which components to select.
Be especially careful of the capacitor characteristics and use X7R or X5R (EIA standard) ceramic capacitors. The capacitance decrease caused by the bias voltage may become large depending on the external size of the capacitor.
- 4) The current limit value is the coil current peak value when switching is not conducted.
The coil current peak value when the actual current limit function begins to operate may exceed the current limit of the electrical characteristics due to the effect of the propagation delay inside the circuit.
- 5) When the On time is less than the Min On Time (t_{ONMIN}) and the dropout voltage is large or the load is low, the PWM control operates intermittently and the ripple voltage may become large or the output voltage may become unstable.
- 6) The ripple voltage could be increased when switching from discontinuous conduction mode to continuous conduction mode and when switching to 100% Duty cycle.
- 7) When the XD9708, PWM/PFM automatic switching type, uses a resistance value of 7.5k Ω or more for R_{F_B2}, ripple may be superimposed due to continuous pulses at high temperature and no load.
To suppress ripple superposition when there is no load, set R_{F_B2} to 7.5k Ω or less, or apply an idle current of 100 μ A or more at no load.
- 8) If the voltage at the EN/SS Pin does not start from 0V but is at the midpoint potential when the power is switched on, the soft start function may not work properly and it may cause larger inrush current and bigger ripple voltages.
- 9) In order to drive the IC normally, supply a stable input voltage to the V_{IN} pin after reducing the AC impedance due to the bypass capacitor. In particular, if the amplitude of the input voltage fluctuates by 5V or more and $\pm 0.1V/\mu s$ or more, there is a possibility that the UVLO function malfunctions due to fluctuations of the internal power supply of the IC.
In that case, switching is stopped in a protected state that prevents false pulse output from the Lx pin. After that, the soft start function gets started, it shifts to normal operation.
If the input voltage fluctuates momentarily, take measures such as increasing the input capacitance.
- 10) Torex places an importance on improving our products and their reliability. We request that users incorporate fail safe designs and post aging protection treatment when using Torex products in their systems.

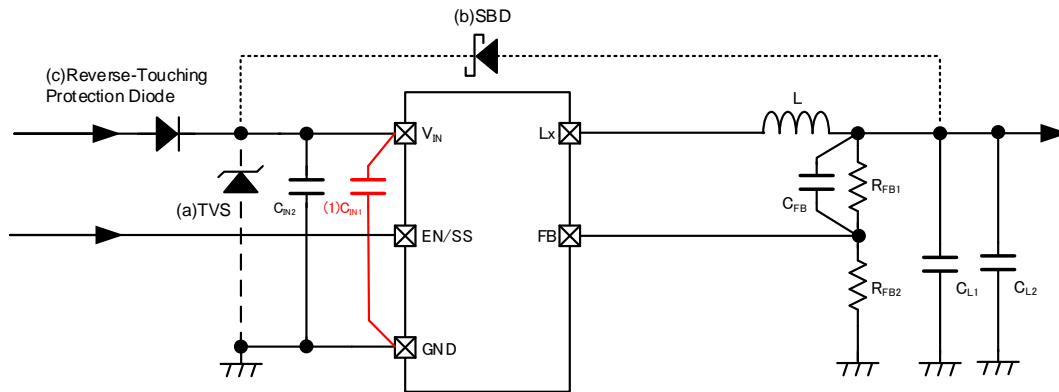
■ **NOTES ON USE (Continued)**

11) Instructions of pattern layouts

The operation may become unstable due to noise and/or phase lag from the output current when the wire impedance is high, please place the input capacitor(C_{IN}) and the output capacitor (C_L) as close to the IC as possible.

(1) In order to stabilize V_{IN} voltage level, we recommend that a by-pass capacitor (C_{IN}) be connected as close as possible to the V_{IN} and GND pins.

If fluctuation of the V_{IN} potential is expected, please take measures such as increasing input capacitor (C_{IN}).



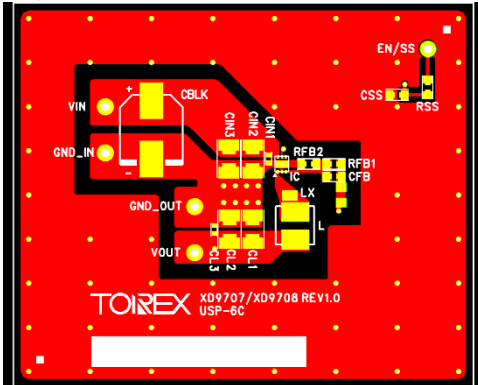
- (2) Please mount each external component as close to the IC as possible.
Please place the external parts on the same side of the PCB as the IC, not on the reverse side of the PCB and elsewhere.
- (3) Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
- (4) Make sure that the GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.
- (5) Please note that internal driver transistors bring on heat because of the load current and ON resistance of High side driver transistor, Low side driver transistor. Please make sure that the heat is dissipated properly, especially at higher temperatures.

NOTE ON USE(Continued)

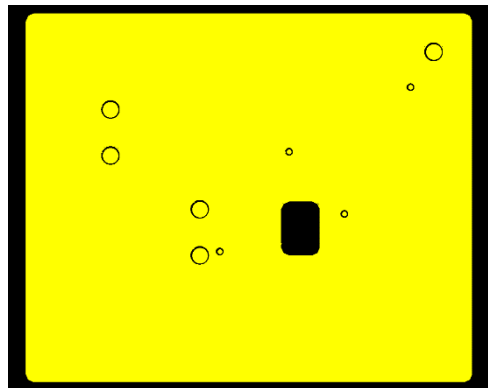
<Reference Pattern Layout>

USP-6C

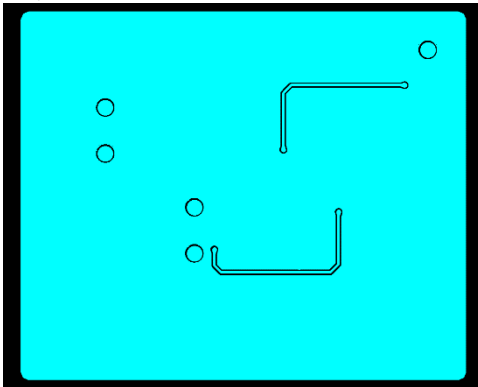
Layer 1



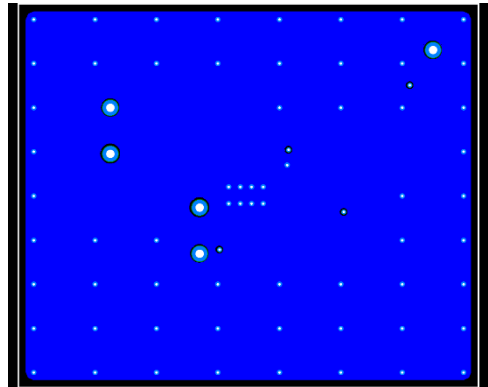
Layer 2



Layer 3

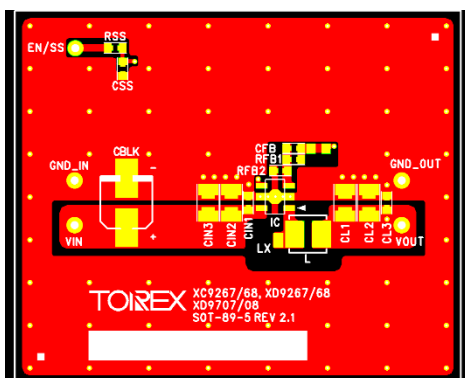


Layer 4

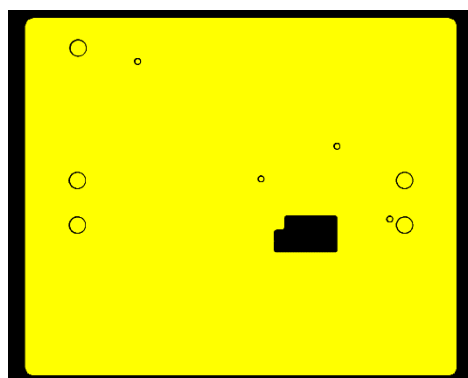


SOT-89-5

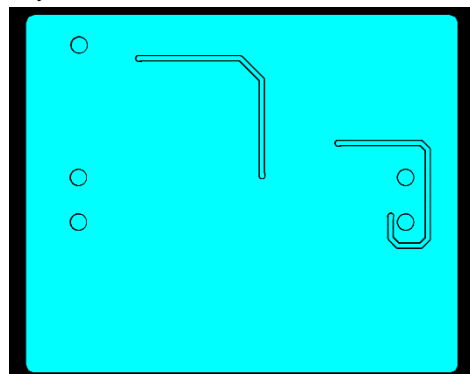
Layer 1



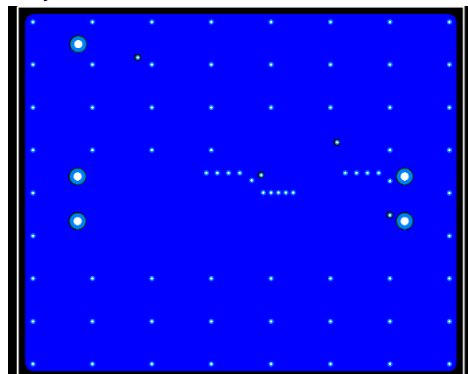
Layer 2



Layer 3

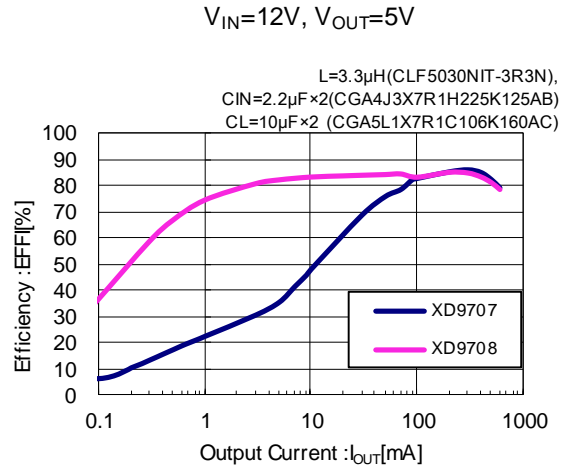
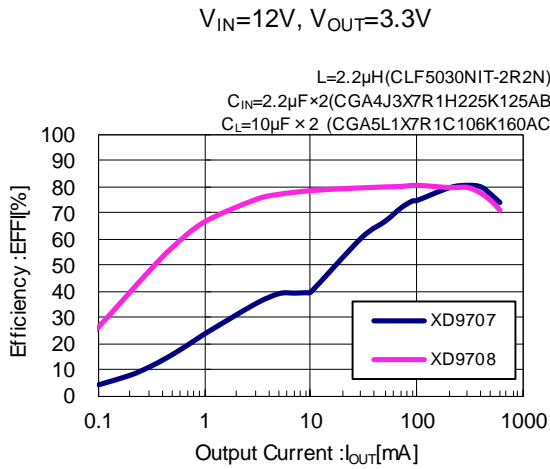


Layer 4

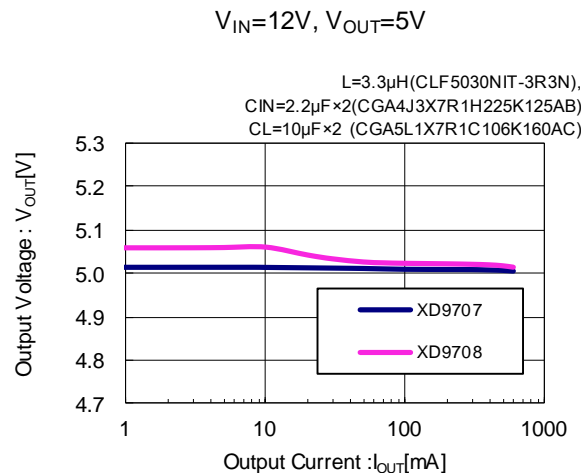
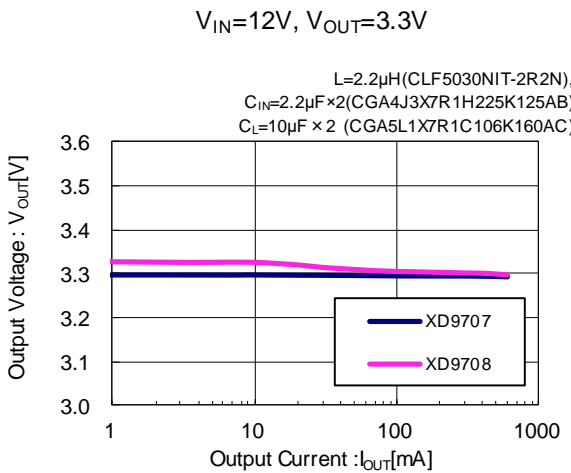


TYPICAL PERFORMANCE CHARACTERISTICS

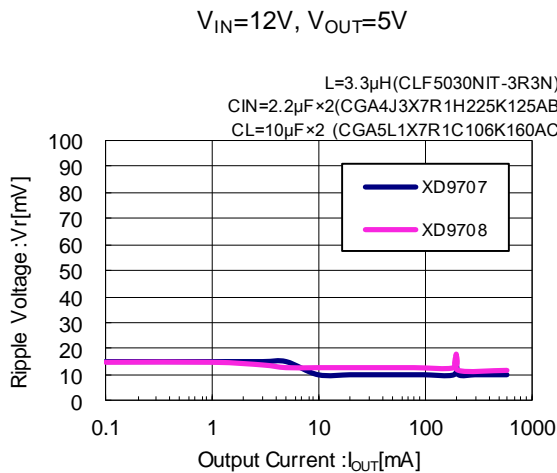
(1) Efficiency vs. Output current



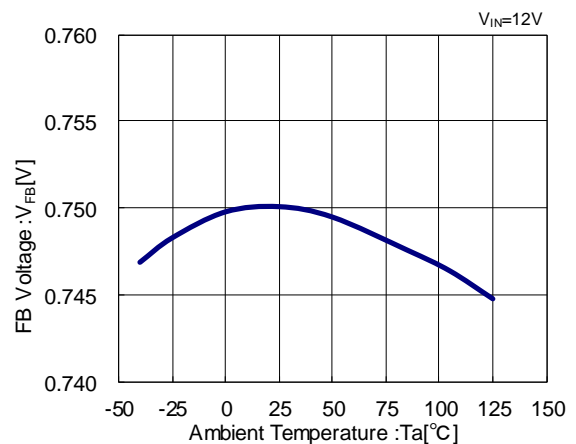
(2) Output Voltage vs. Output Current



(3) Ripple Voltage vs. Output Current

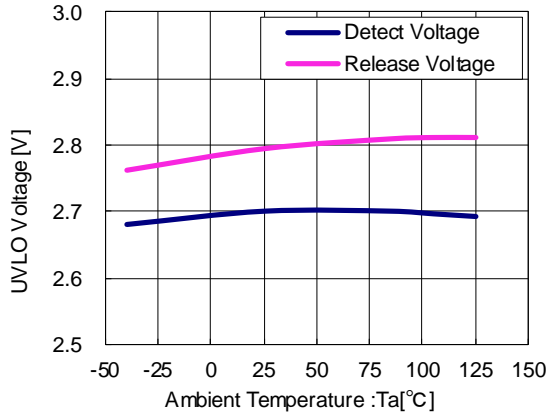


(4) FB Voltage vs. Ambient Temperature

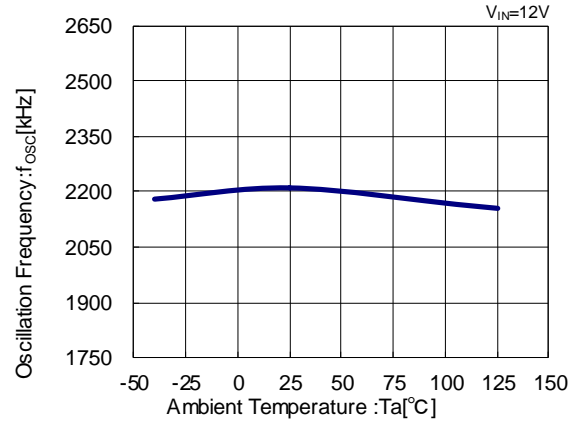


TYPICAL PERFORMANCE CHARACTERISTICS

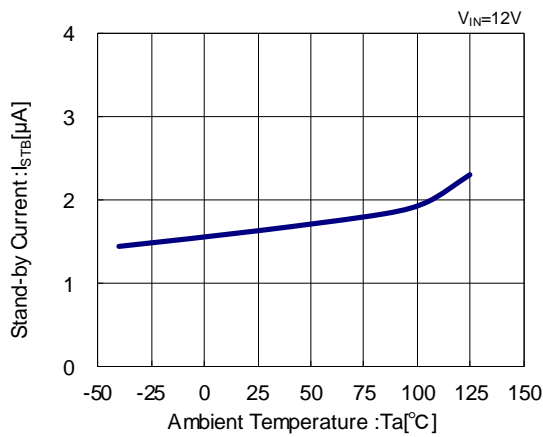
(5) UVLO Voltage vs. Ambient Temperature



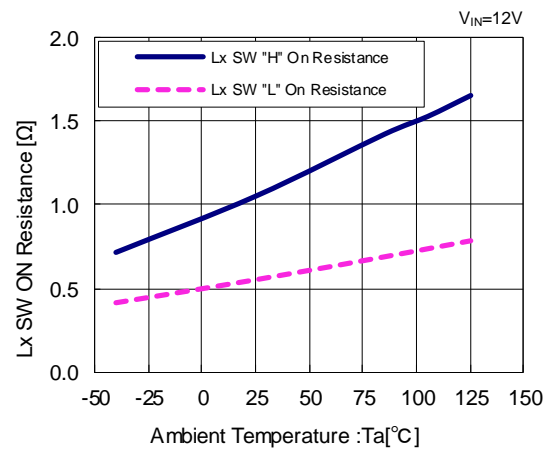
(6) Oscillation Frequency vs. Ambient Temperature



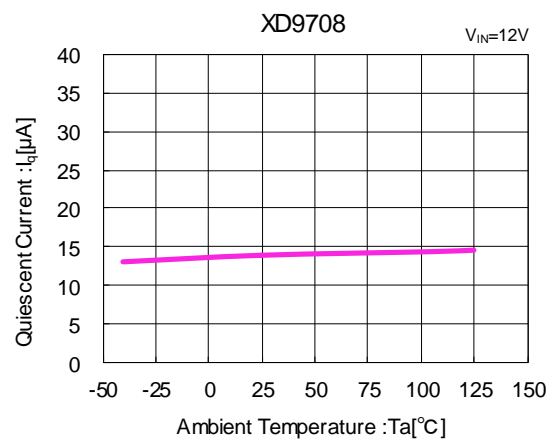
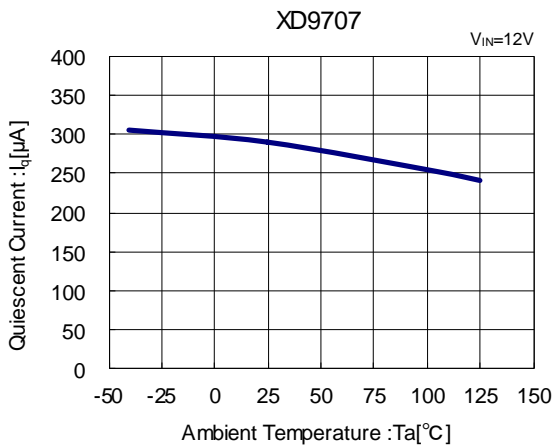
(7) Stand-by Current vs. Ambient Temperature



(8) Lx SW ON Resistance vs. Ambient Temperature

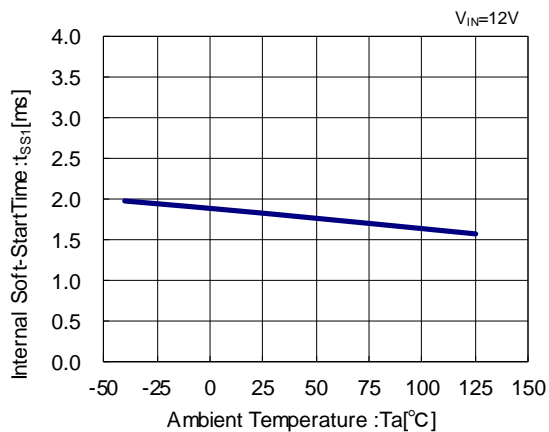


(9) Quiescent Current vs. Ambient Temperature

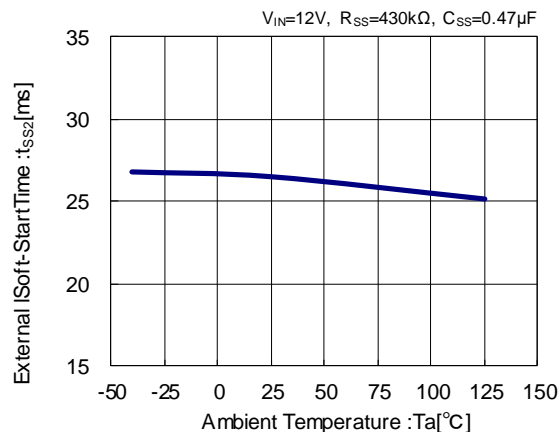


TYPICAL PERFORMANCE CHARACTERISTICS

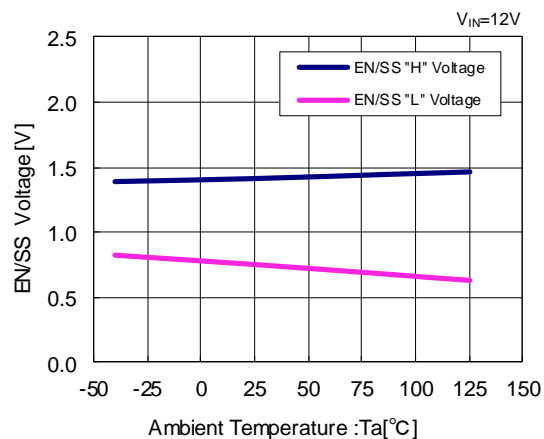
(10) Internal Soft-Start Time vs. Ambient Temperature



(11) External Soft-Start Time vs. Ambient Temperature

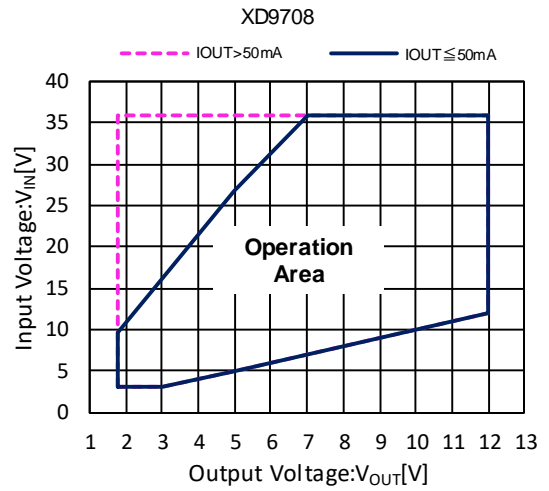
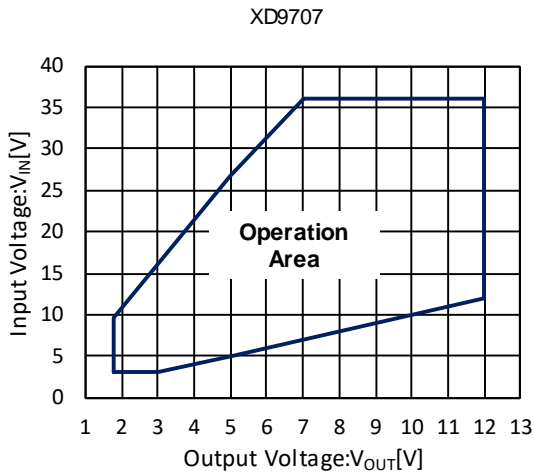


(12) EN/SS Voltage vs. Ambient Temperature

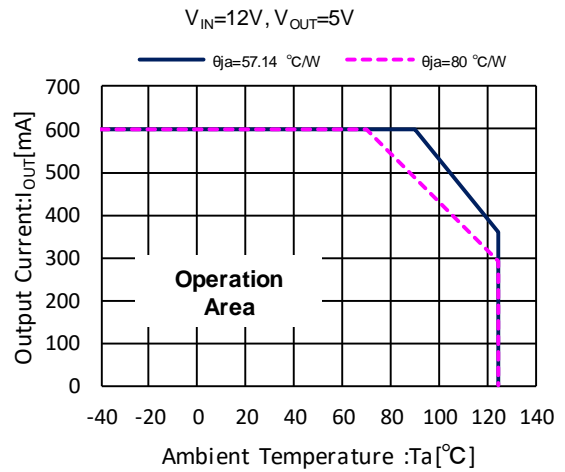
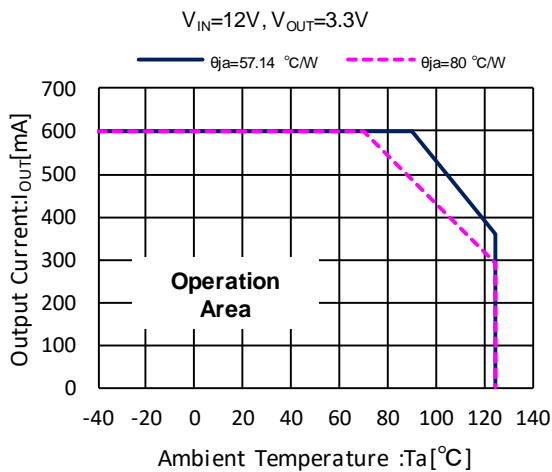


TYPICAL PERFORMANCE CHARACTERISTICS

(13) V_{IN} - V_{OUT} Operation Area

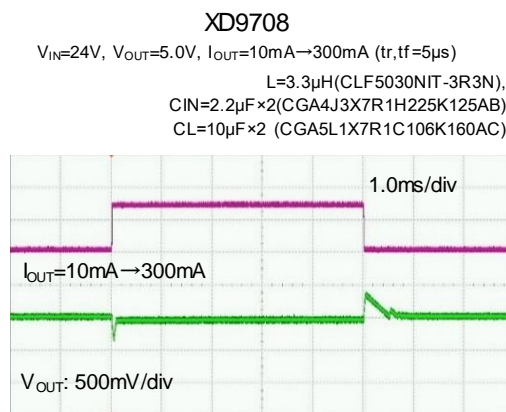
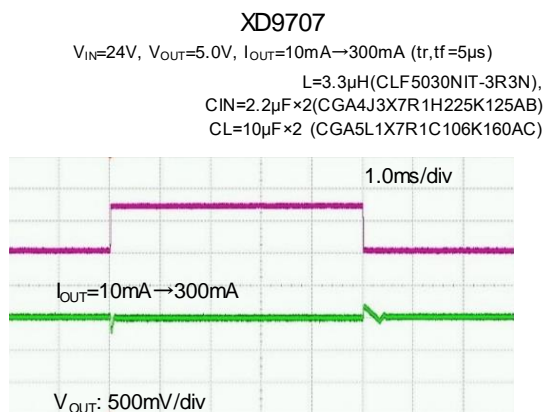
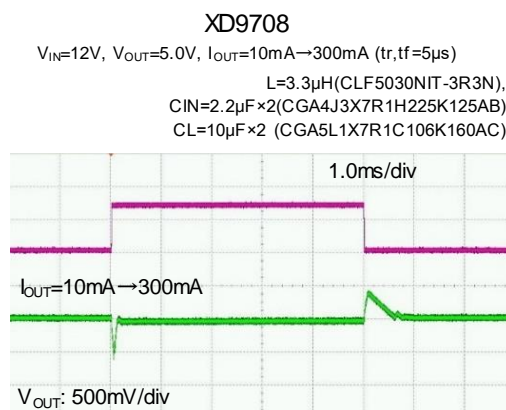
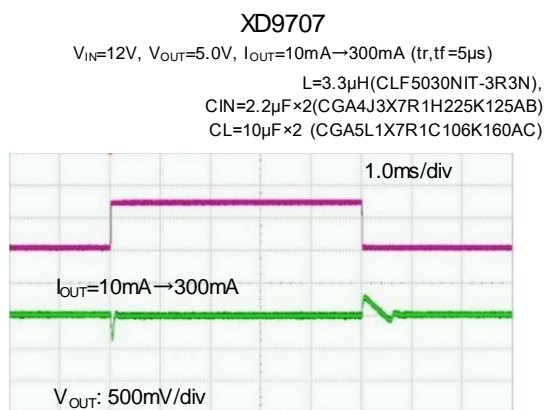
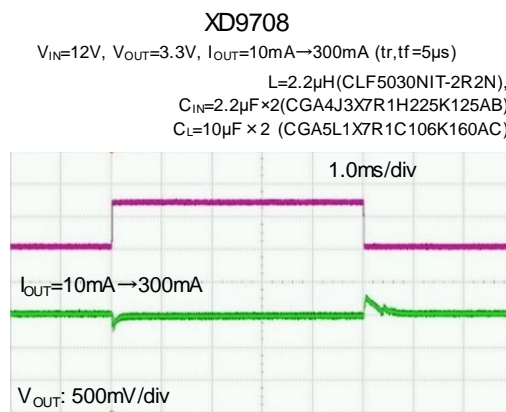
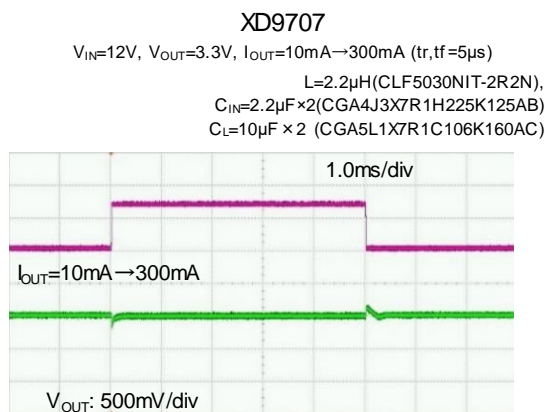


(14) Output Current Operation Area



TYPICAL PERFORMANCE CHARACTERISTICS

(15) Load Transient Response

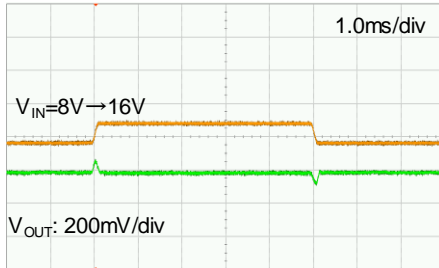


TYPICAL PERFORMANCE CHARACTERISTICS

(16) Input Transient Response

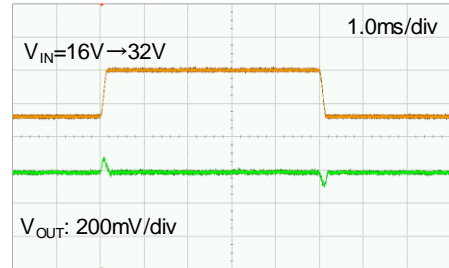
$V_{IN}=8V \rightarrow 16V$, $V_{OUT}=5.0V$, $I_{OUT}=300mA$ ($t_r, t_f=100\mu s$)

$L=3.3\mu H$ (CLF5030NIT-3R3N),
 $C_{IN}=2.2\mu F \times 2$ (CGA4J3X7R1H225K125AB)
 $C_L=10\mu F \times 2$ (CGA5L1X7R1C106K160AC)



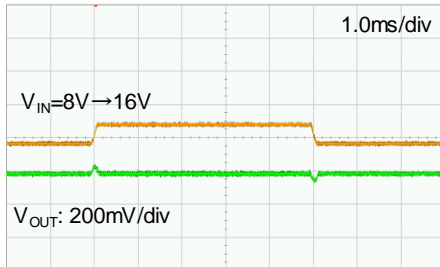
$V_{IN}=16V \rightarrow 32V$, $V_{OUT}=5.0V$, $I_{OUT}=300mA$ ($t_r, t_f=100\mu s$)

$L=3.3\mu H$ (CLF5030NIT-3R3N),
 $C_{IN}=2.2\mu F \times 2$ (CGA4J3X7R1H225K125AB)
 $C_L=10\mu F \times 2$ (CGA5L1X7R1C106K160AC)



$V_{IN}=8V \rightarrow 16V$, $V_{OUT}=3.3V$, $I_{OUT}=300mA$ ($t_r, t_f=100\mu s$)

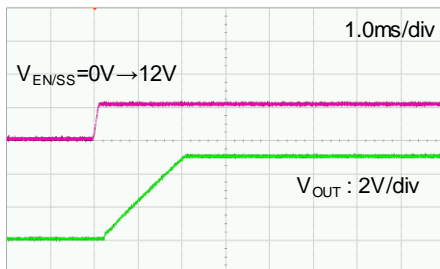
$L=2.2\mu H$ (CLF5030NIT-2R2N),
 $C_{IN}=2.2\mu F \times 2$ (CGA4J3X7R1H225K125AB)
 $C_L=10\mu F \times 2$ (CGA5L1X7R1C106K160AC)



(17) EN/SS Rising Response

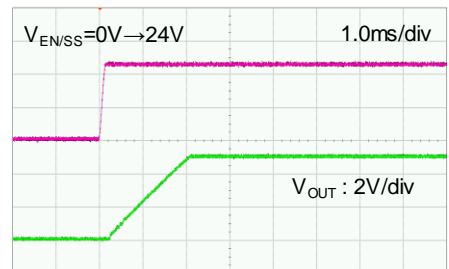
$V_{IN}=12V$, $V_{EN/SS}=0V \rightarrow 12V$, $V_{OUT}=5V$, $I_{OUT}=300mA$

$L=3.3\mu H$ (CLF5030NIT-3R3N),
 $C_{IN}=2.2\mu F \times 2$ (CGA4J3X7R1H225K125AB)
 $C_L=10\mu F \times 2$ (CGA5L1X7R1C106K160AC)



$V_{IN}=24V$, $V_{EN/SS}=0V \rightarrow 24V$, $V_{OUT}=5V$, $I_{OUT}=300mA$

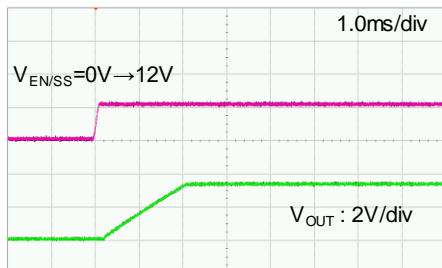
$L=3.3\mu H$ (CLF5030NIT-3R3N),
 $C_{IN}=2.2\mu F \times 2$ (CGA4J3X7R1H225K125AB)
 $C_L=10\mu F \times 2$ (CGA5L1X7R1C106K160AC)



TYPICAL PERFORMANCE CHARACTERISTICS

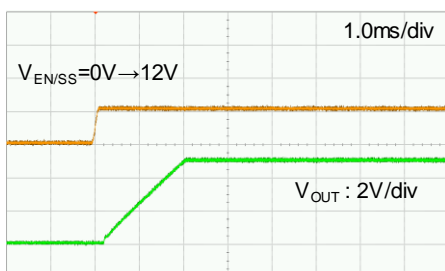
(17) EN/SS Rising Response

$V_{IN}=12V, V_{EN/SS}=0V \rightarrow 12V, V_{OUT}=3.3V, I_{OUT}=300mA$
 $L=2.2\mu H$ (CLF5030NIT-2R2N),
 $C_{IN}=2.2\mu F \times 2$ (CGA4J3X7R1H225K125AB)
 $C_L=10\mu F \times 2$ (CGA5L1X7R1C106K160AC)

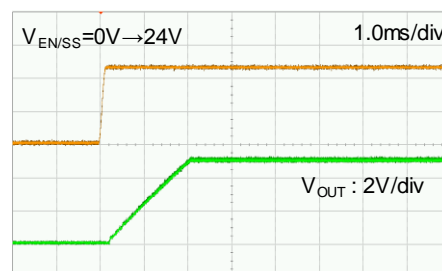


(18) V_{IN} Rising Response

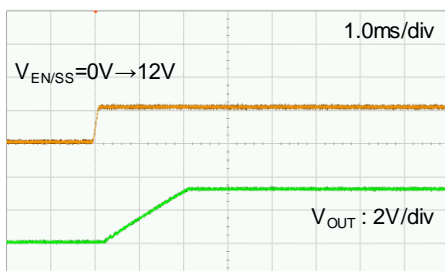
$V_{IN}=0V \rightarrow 12V, V_{EN/SS}=0V \rightarrow 12V, V_{OUT}=5V, I_{OUT}=300mA$
 $L=3.3\mu H$ (CLF5030NIT-3R3N),
 $C_{IN}=2.2\mu F \times 2$ (CGA4J3X7R1H225K125AB)
 $C_L=10\mu F \times 2$ (CGA5L1X7R1C106K160AC)



$V_{IN}=0V \rightarrow 24V, V_{EN/SS}=0V \rightarrow 24V, V_{OUT}=5V, I_{OUT}=300mA$
 $L=3.3\mu H$ (CLF5030NIT-3R3N),
 $C_{IN}=2.2\mu F \times 2$ (CGA4J3X7R1H225K125AB)
 $C_L=10\mu F \times 2$ (CGA5L1X7R1C106K160AC)



$V_{IN}=0V \rightarrow 12V, V_{EN/SS}=0V \rightarrow 12V, V_{OUT}=3.3V, I_{OUT}=300mA$
 $L=2.2\mu H$ (CLF5030NIT-2R2N),
 $C_{IN}=2.2\mu F \times 2$ (CGA4J3X7R1H225K125AB)
 $C_L=10\mu F \times 2$ (CGA5L1X7R1C106K160AC)



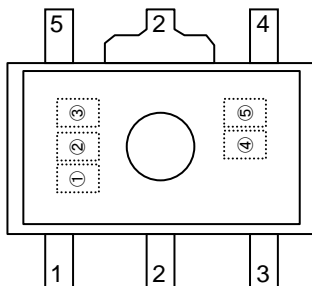
■ PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
SOT-89-5	SOT-89-5 PKG	SOT-89-5 Power Dissipation
USP-6C	USP-6C PKG	USP-6C Power Dissipation

MARKING RULE

● SOT-89-5

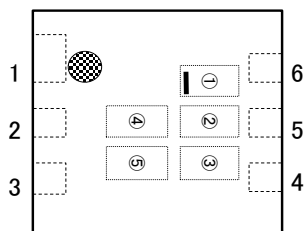


①② represents product series, products type

MARK		PRODUCT SERIES
①	②	
K	1	XD9707B75***-Q
	2	XD9708B75***-Q

※USP-6C with underline mark

● USP-6C(with underline mark)



③ presents Oscillation Frequency

MARK	Oscillation Frequency	PRODUCT SERIES
T	2.2MHz	XD970*B75D**-Q

④⑤ represents production lot number
01~09, 0A~0Z, 11~9Z, A1~A9, AA~AZ, B1~ZZ repeated
(G, I, J, O, Q, W excluded)* No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.
2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.
3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.
4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions, excluding when specified for in-vehicle use or other uses.
Do not use the product for in-vehicle use or other uses unless agreed by us in writing in advance.
5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.
6. Our products are not designed to be Radiation-resistant.
7. Please use the product listed in this datasheet within the specified ranges.
8. We assume no responsibility for damage or loss due to abnormal use.
9. All rights reserved. No part of this datasheet may be copied or reproduced unless agreed by Torex Semiconductor Ltd in writing in advance.

TOREX SEMICONDUCTOR LTD.